

PG132-A02

370W, FH Std PCB, 384b, GDDR6x 2CH X16  
DP + DP + DP + HDMI/DP

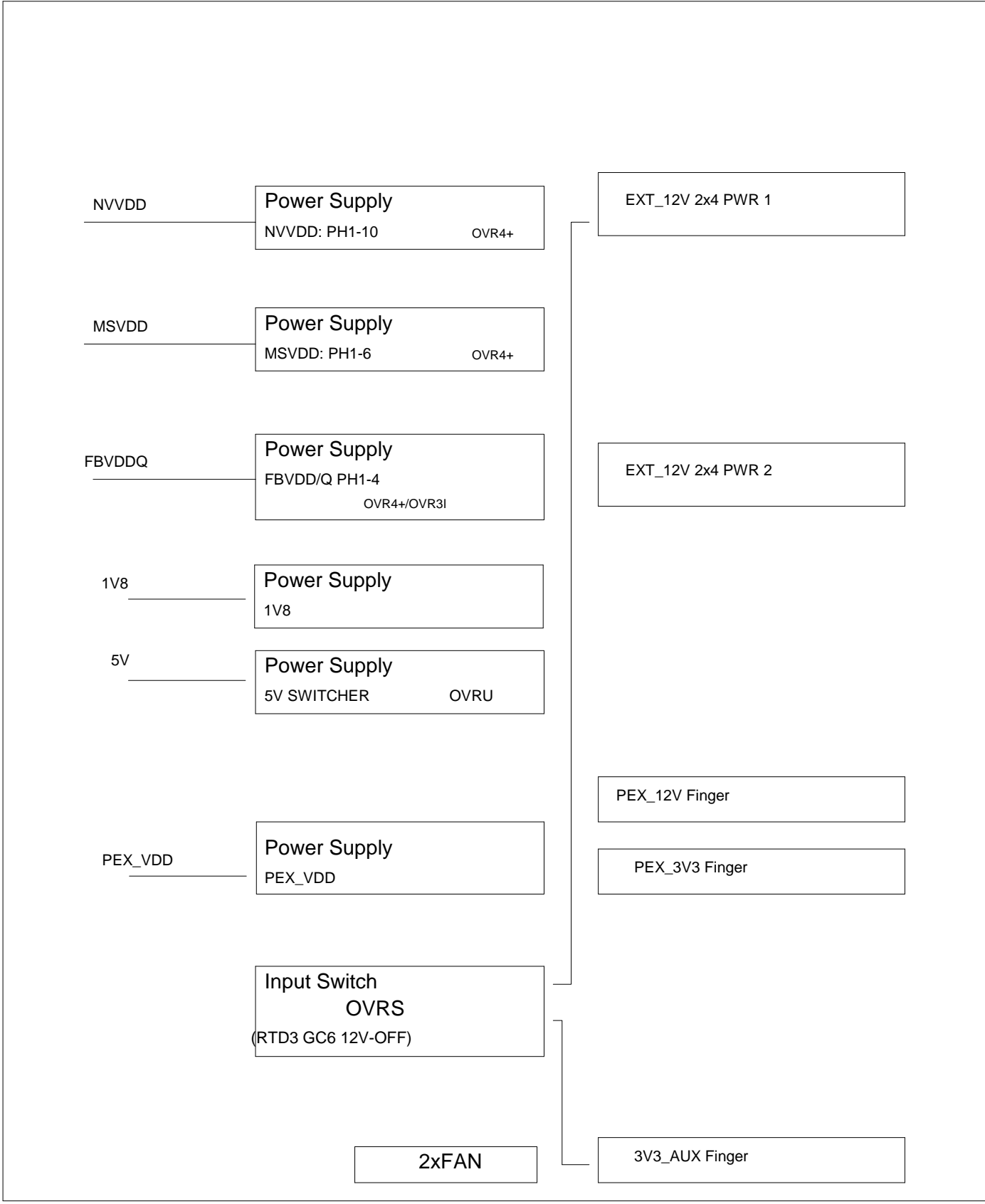
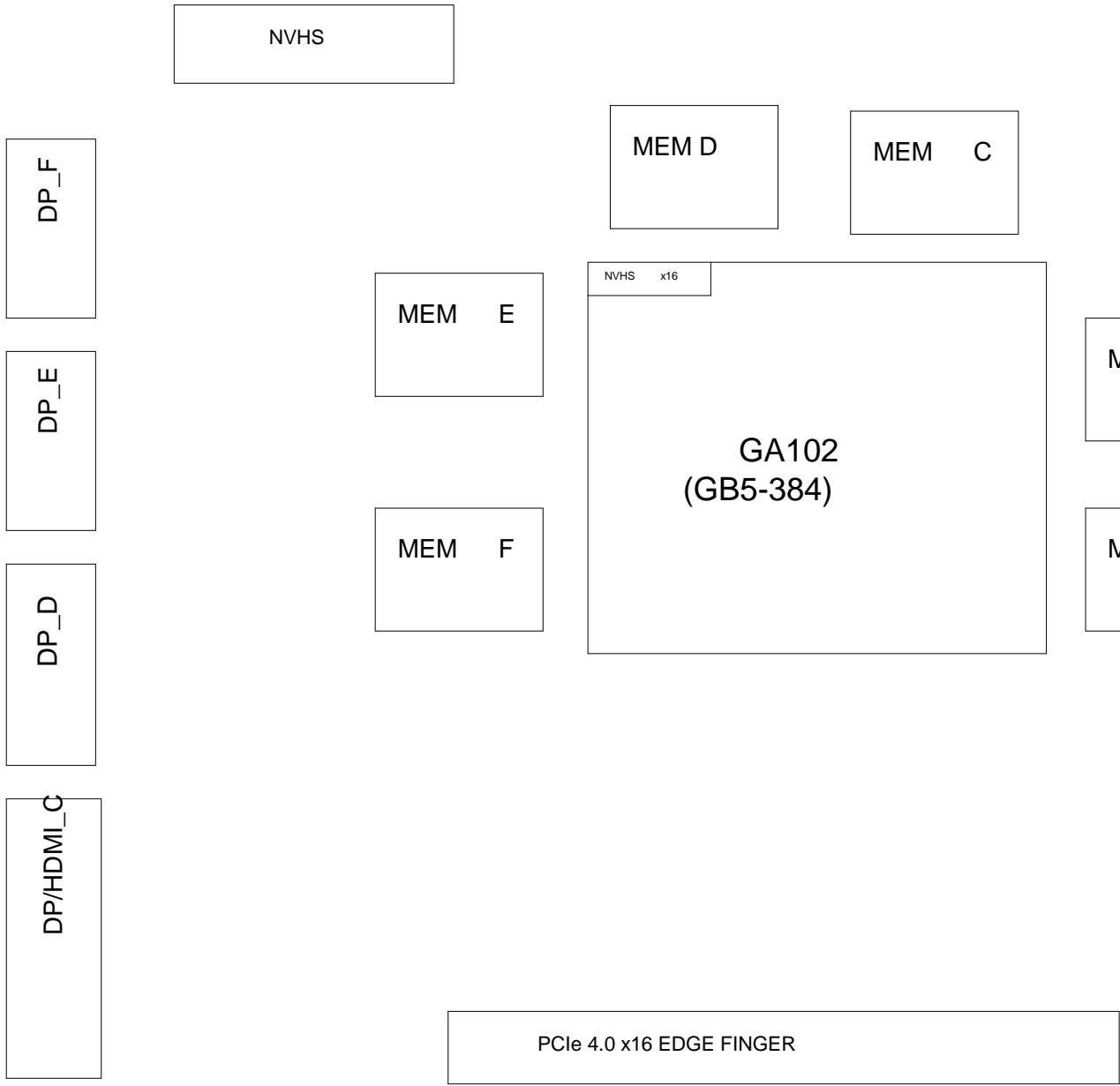
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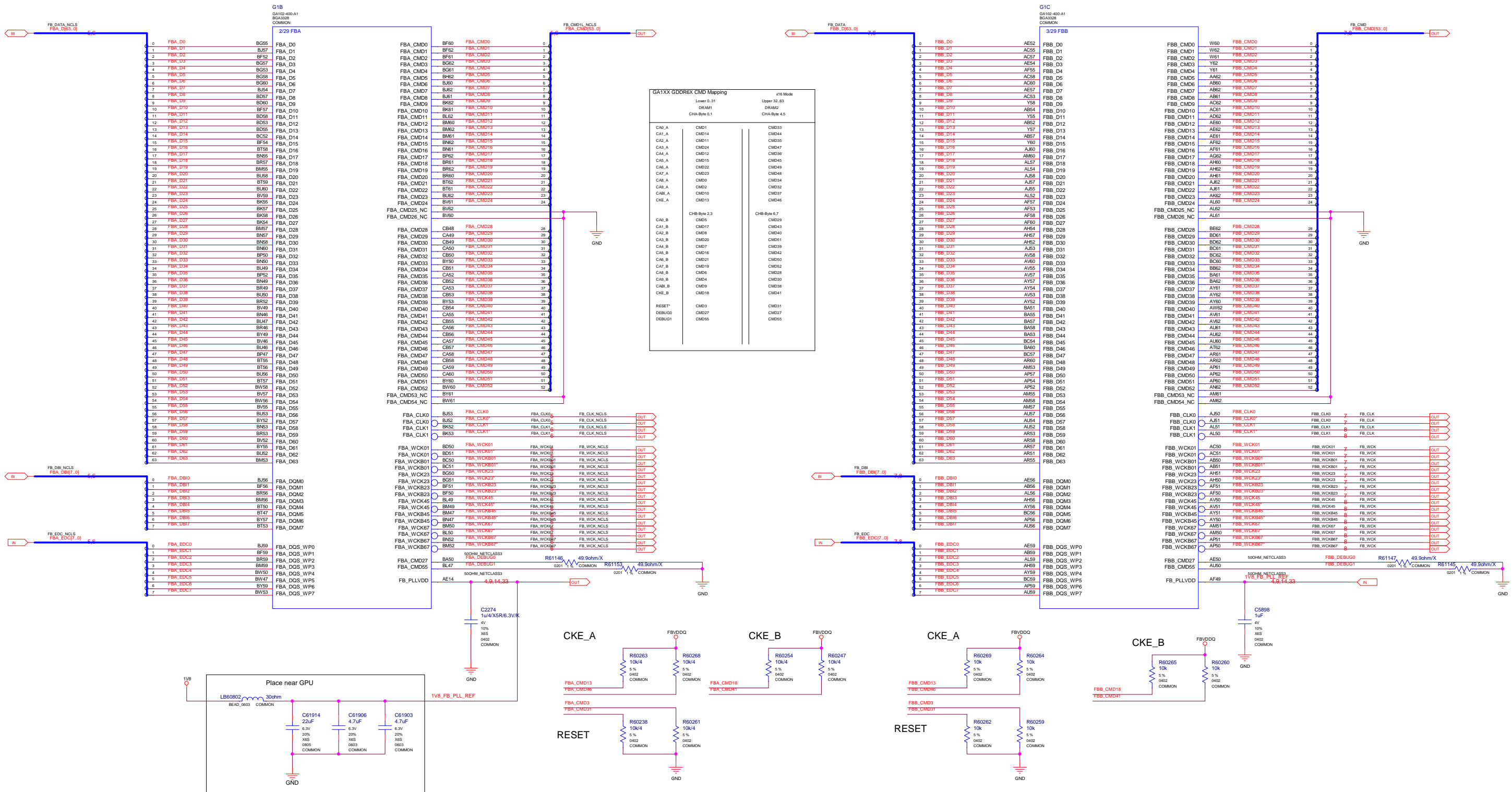
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52	PS: NVVDD Controller_OVR8
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Block Diagram

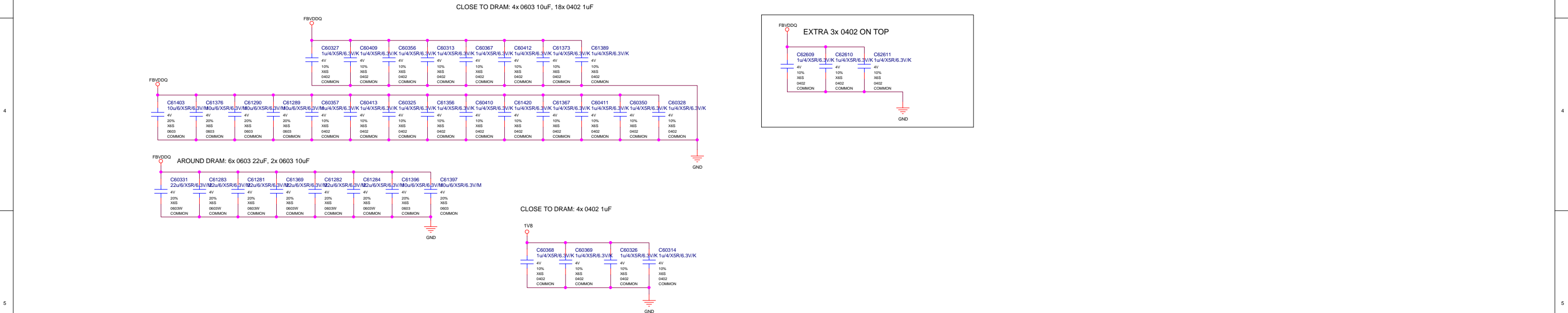
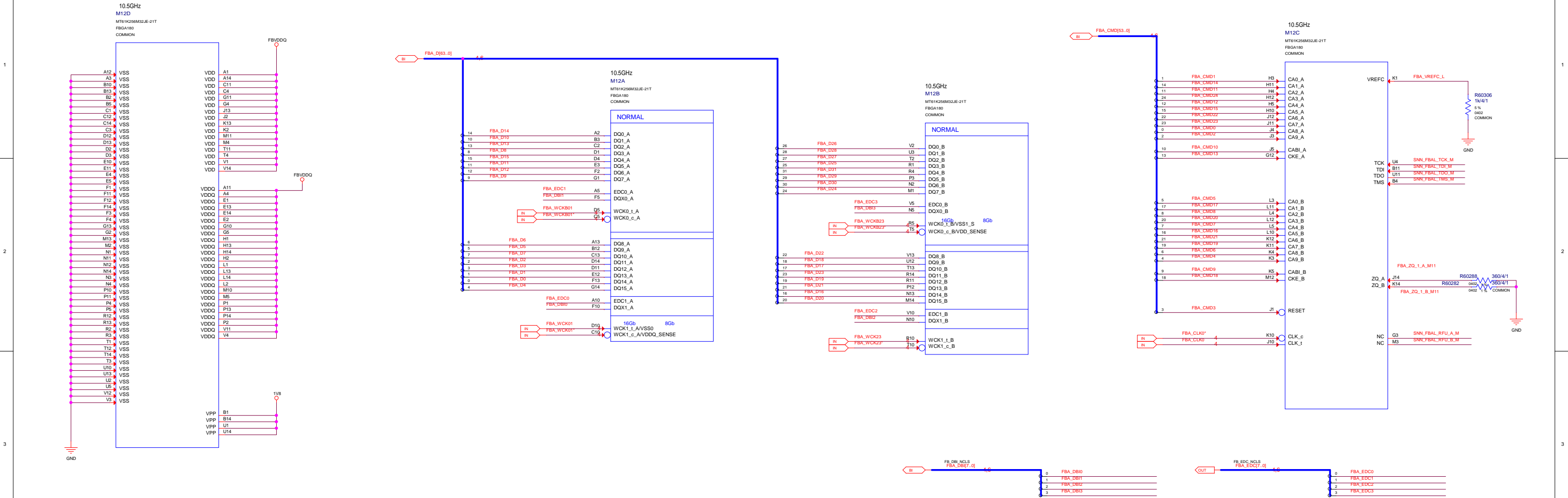




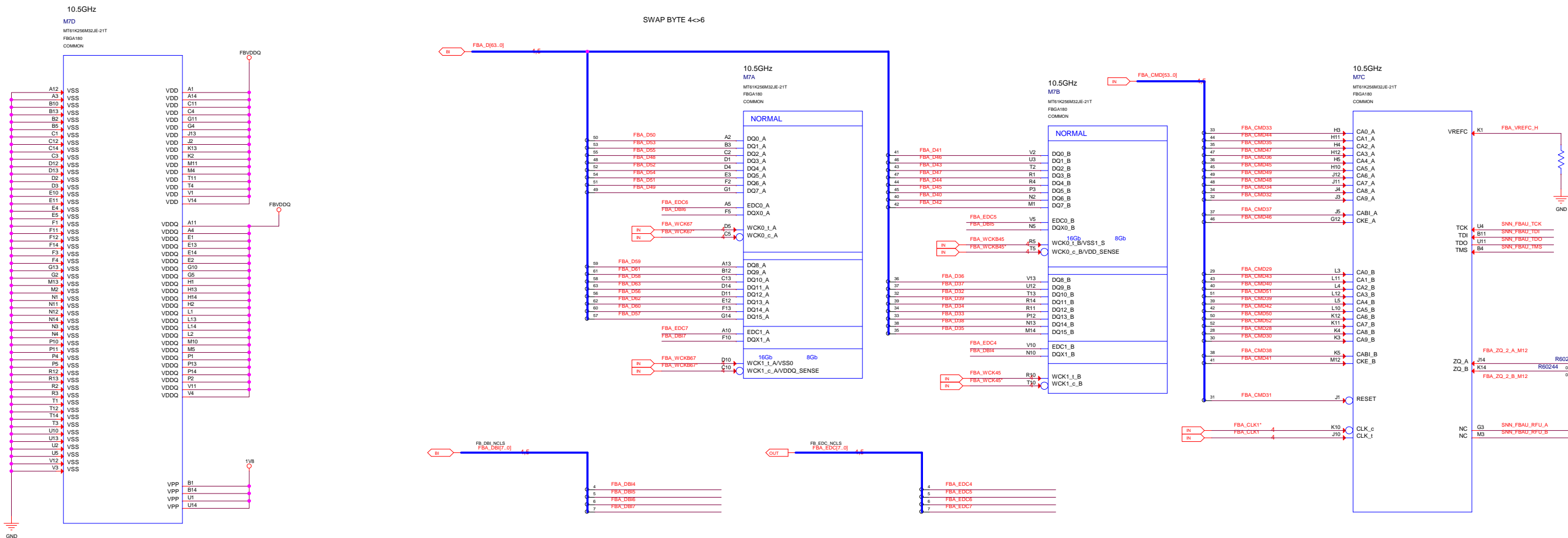
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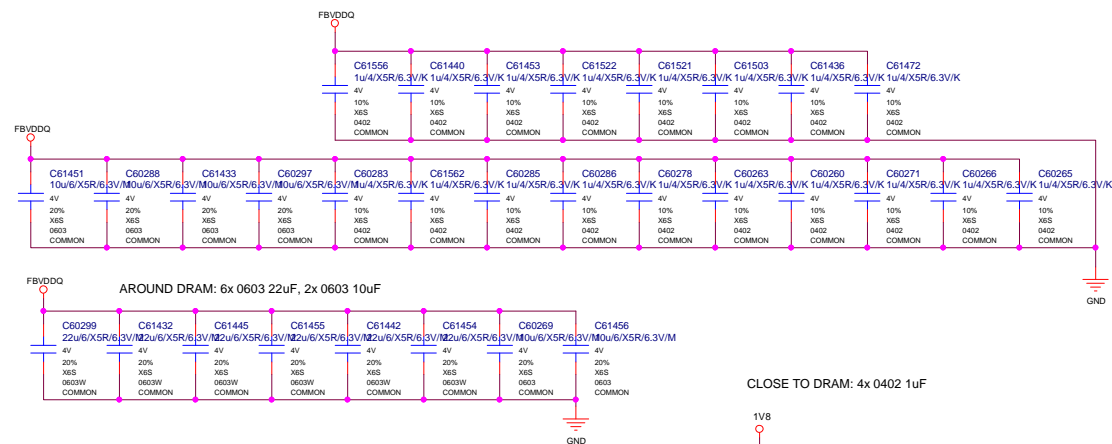
MEMORY: FBA Partition 31..0



MEMORY: FBA Partition 63..32



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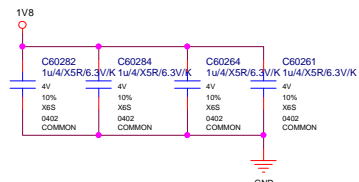


AROUND DRAM: 6x 0603 22uF, 2x 0603 10uF

EXTRA 1x 0402 ON BOT



CLOSE TO DRAM: 4x 0402 1uF



ASSEMBLY  
PAGE DETAIL

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MEMORY: FBA PARTITION[63:32]
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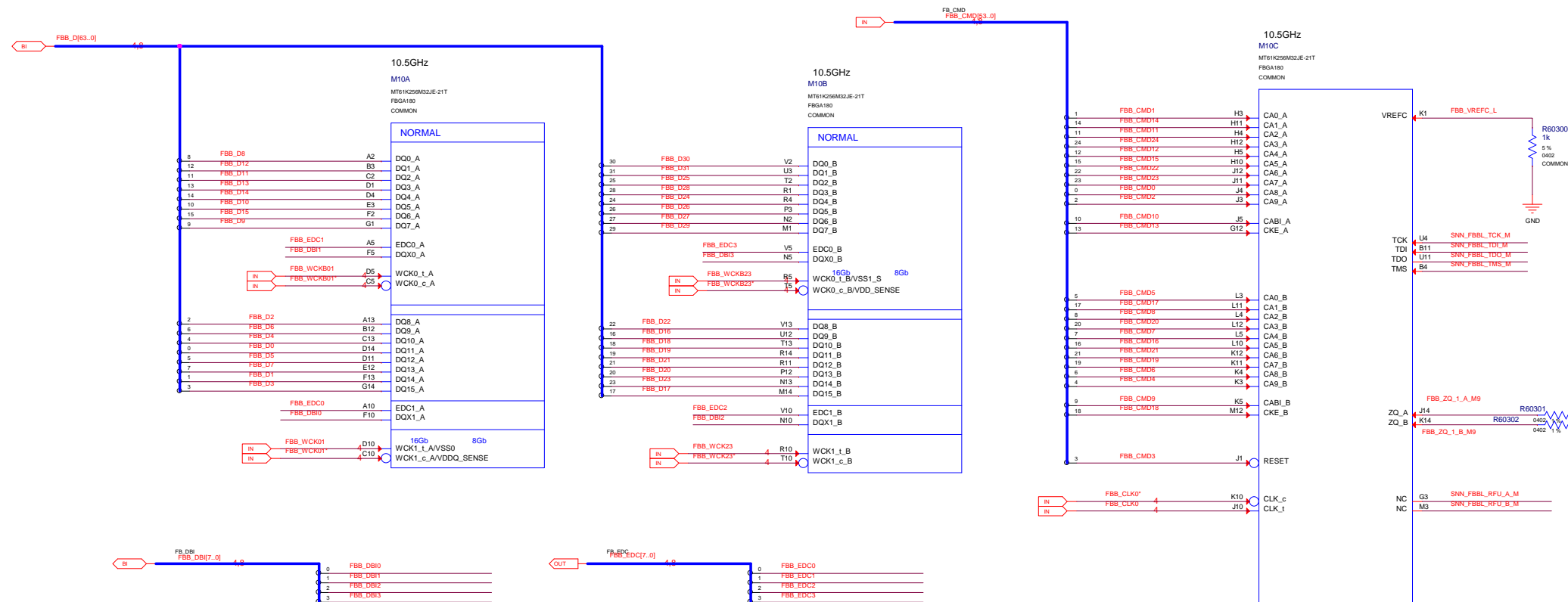
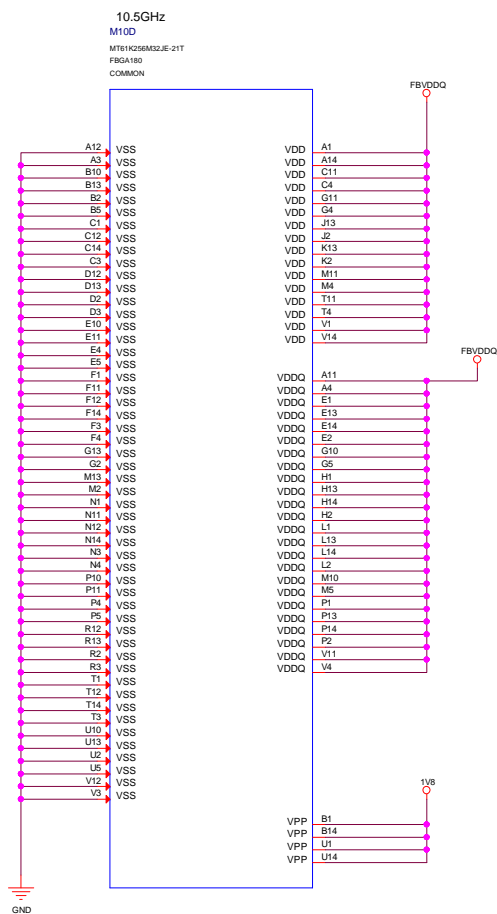
## GIGABYTE

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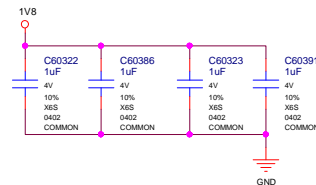
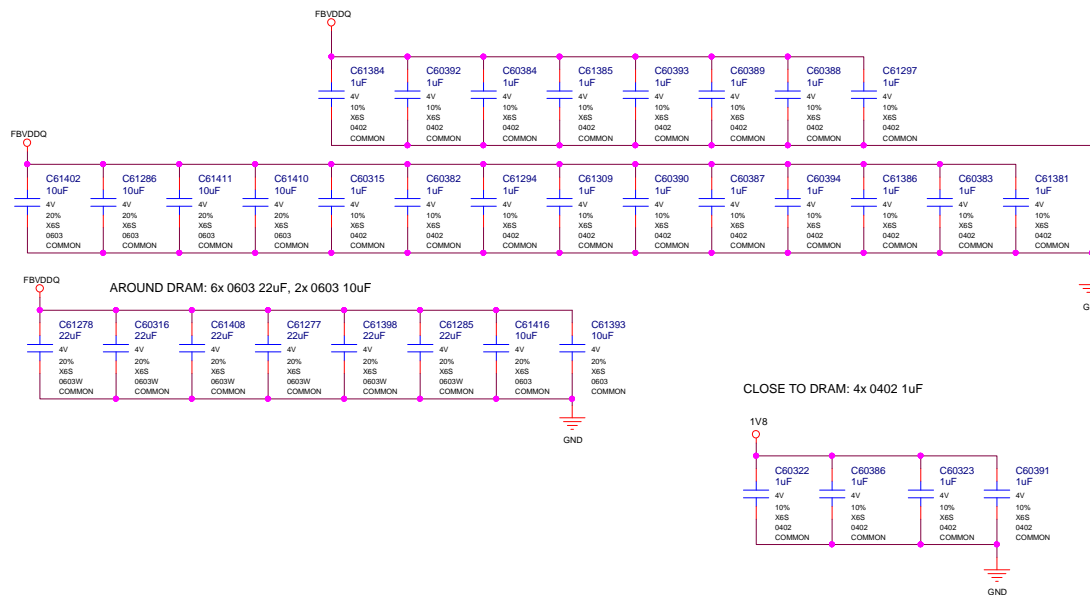
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GV-NS080A0R05 X-10GD  
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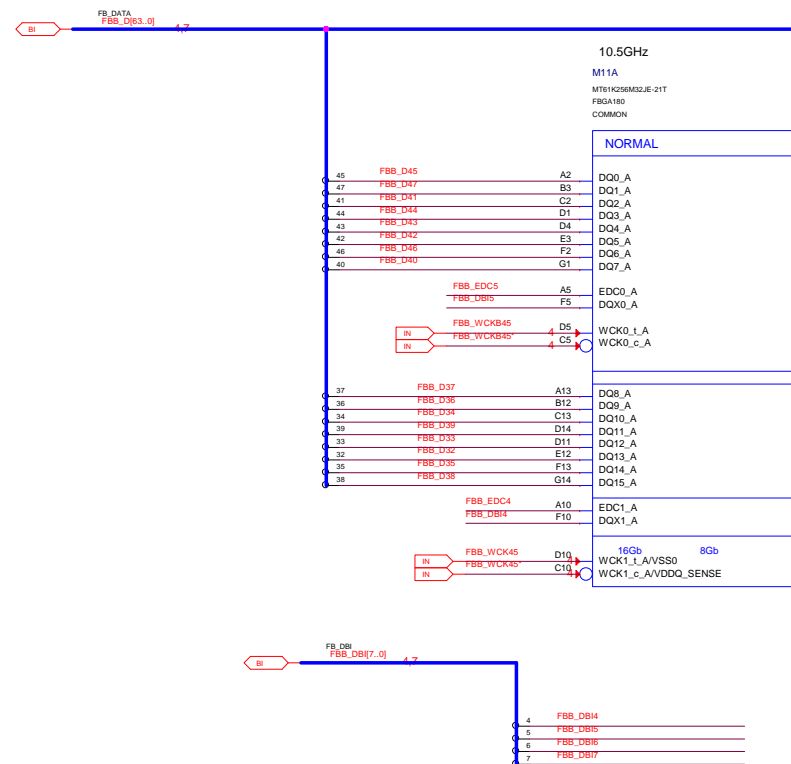
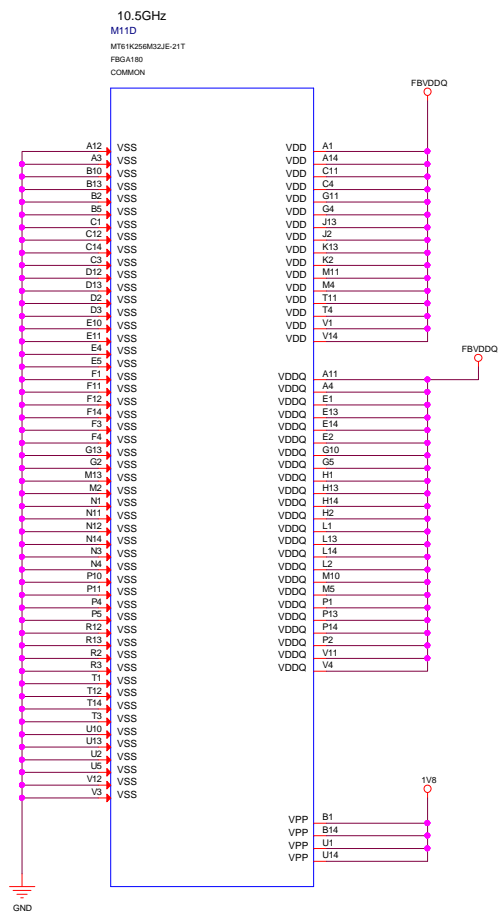


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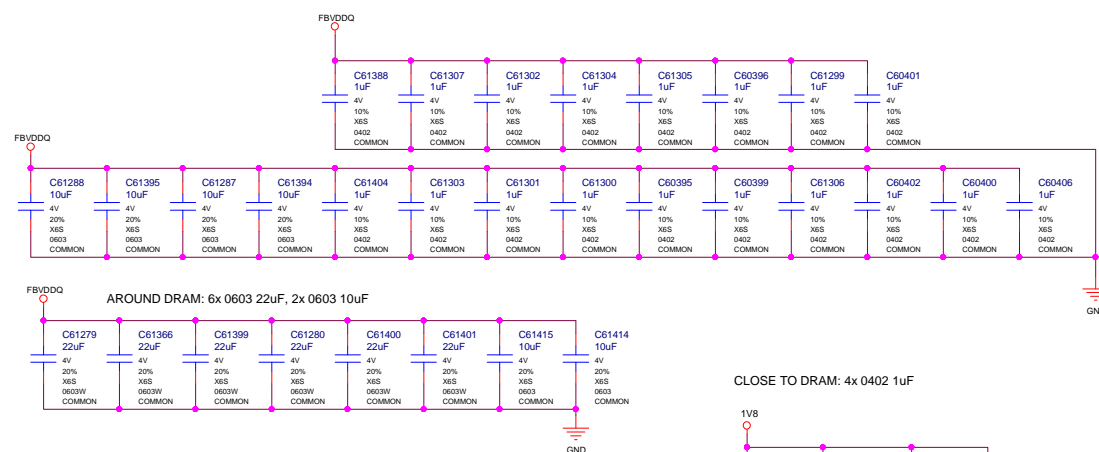
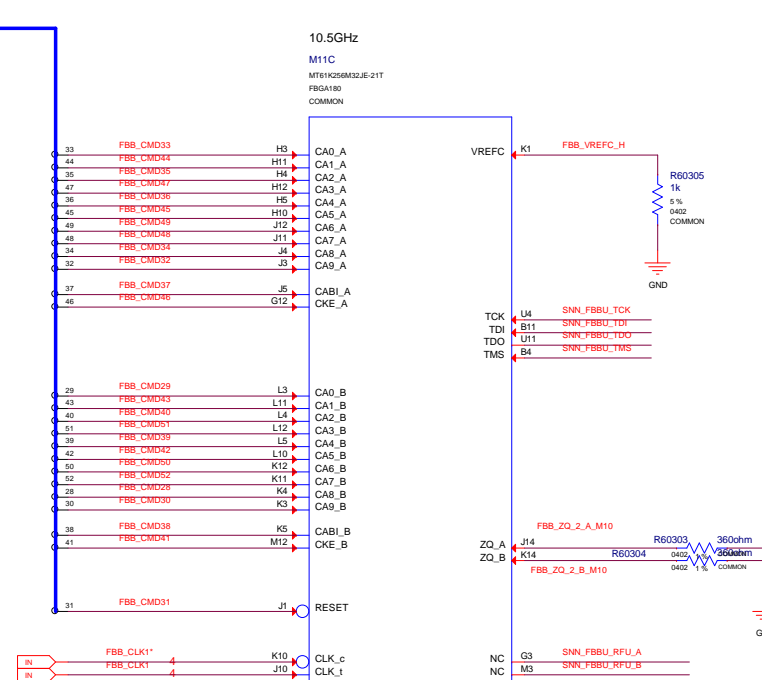
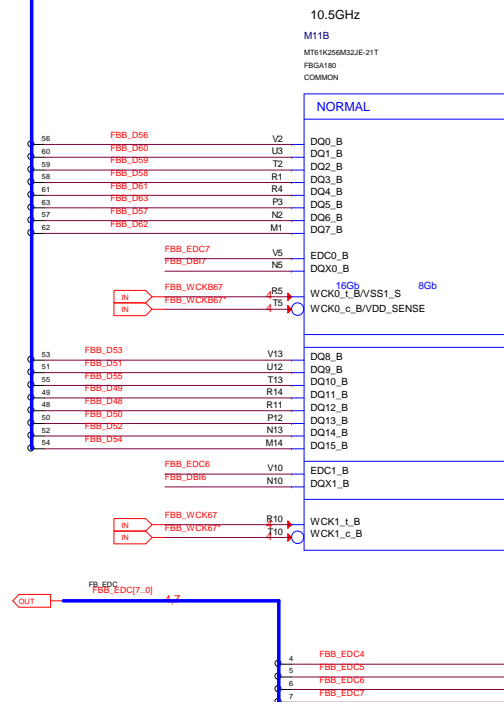




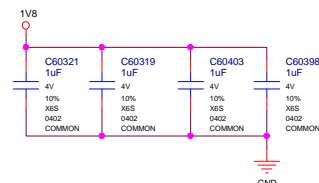
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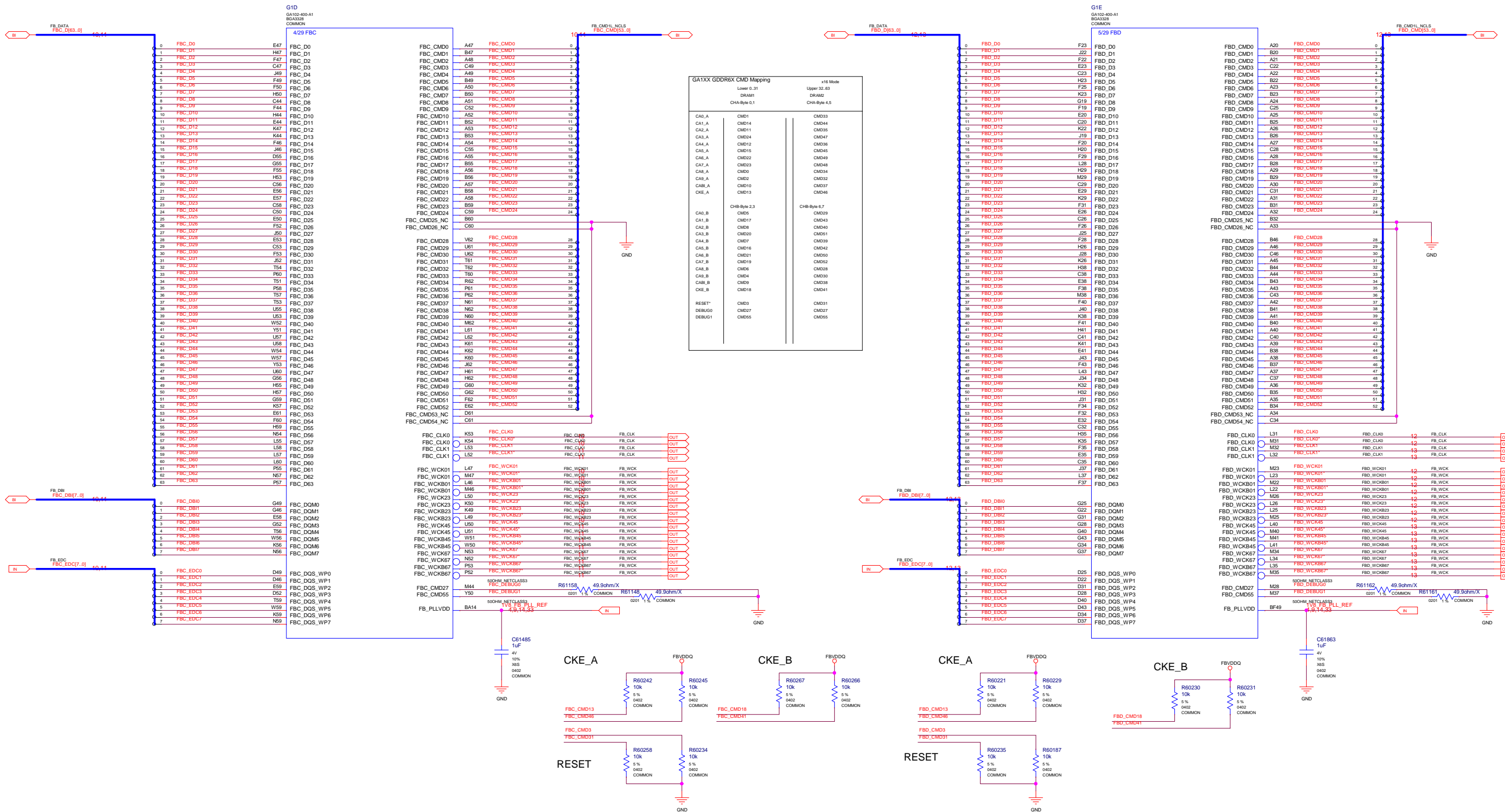


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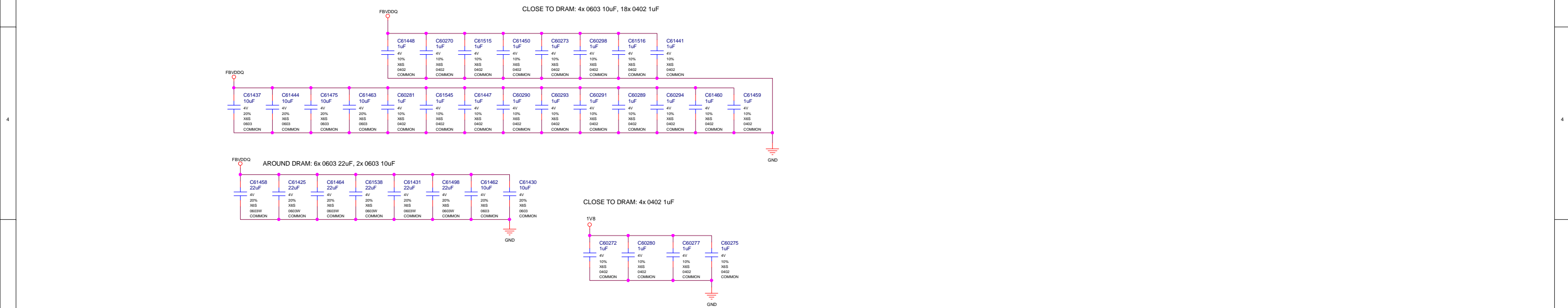
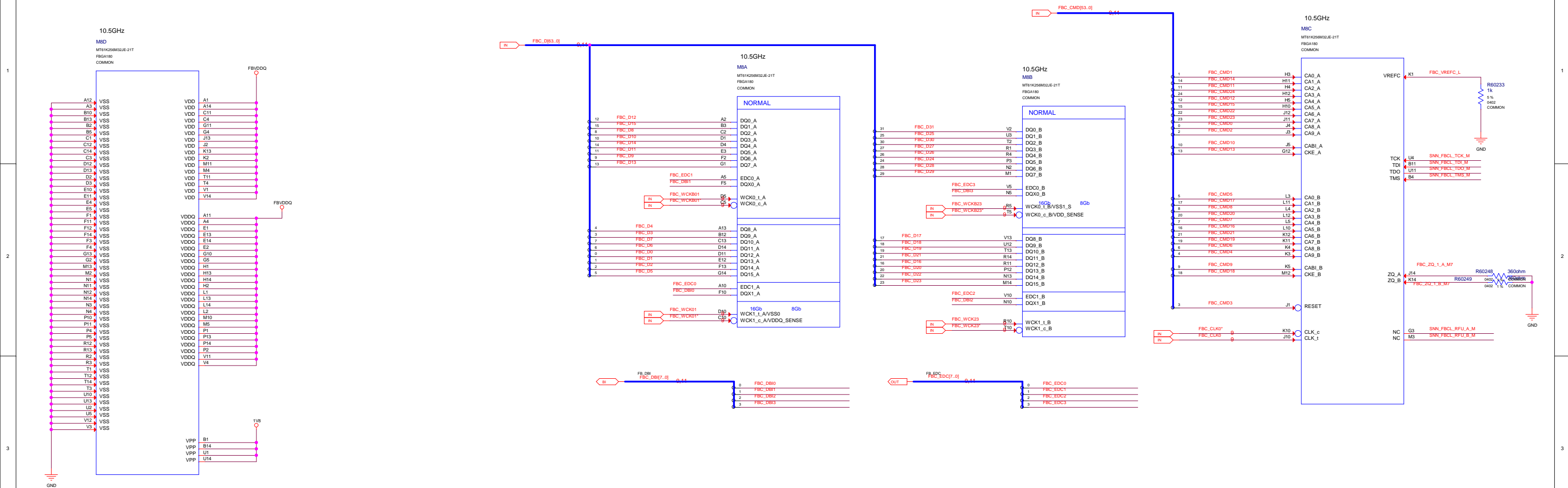




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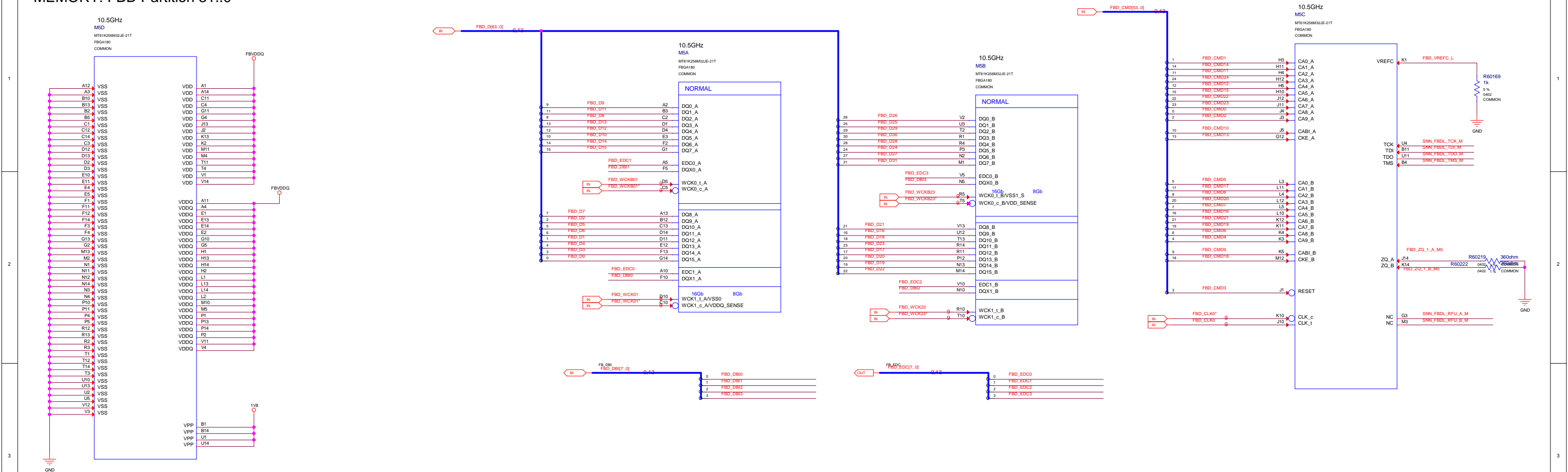


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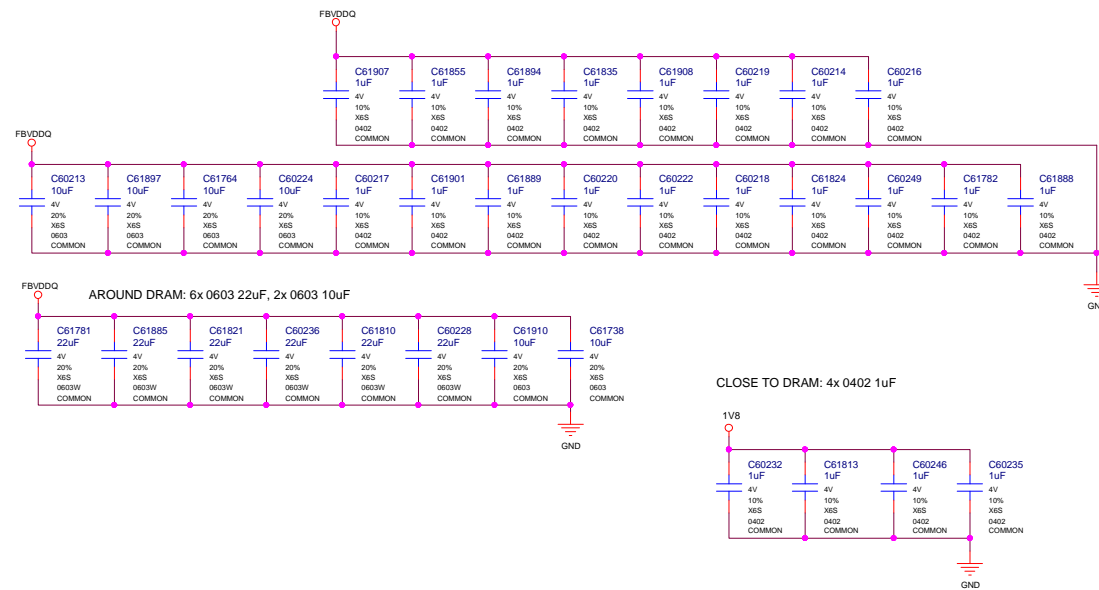




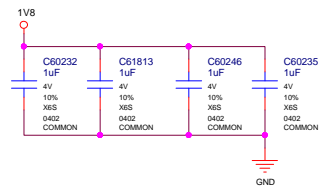
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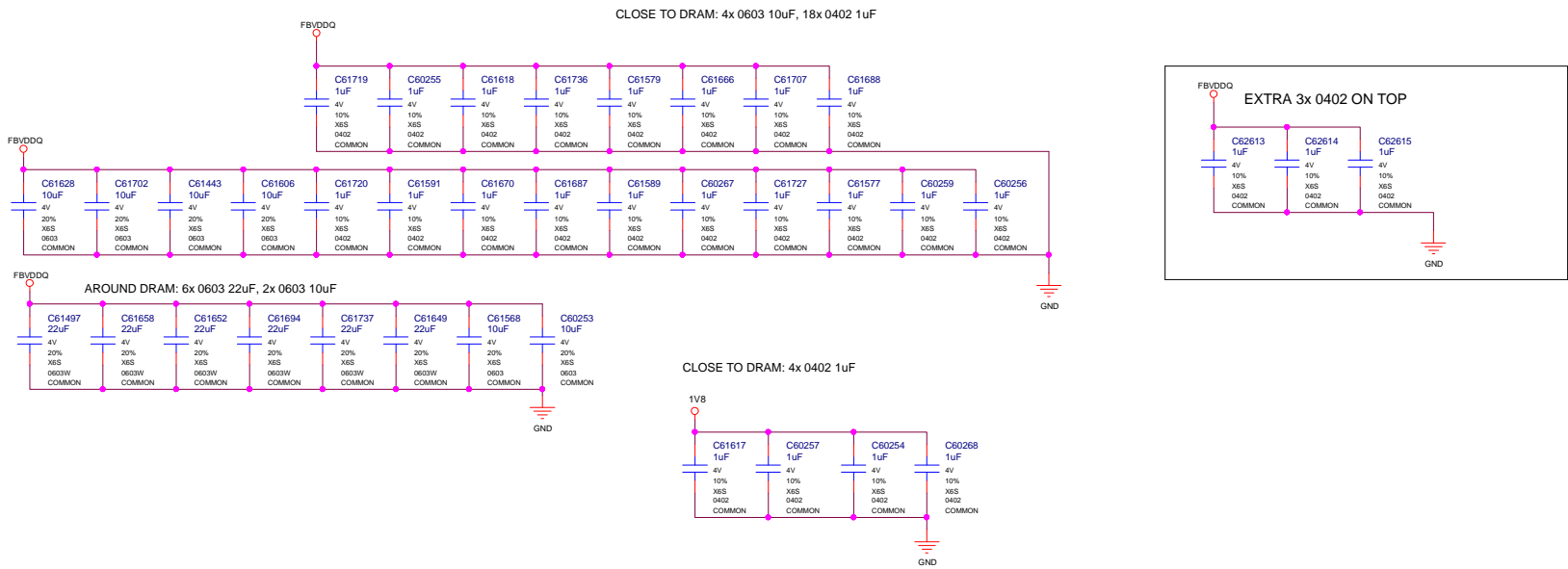
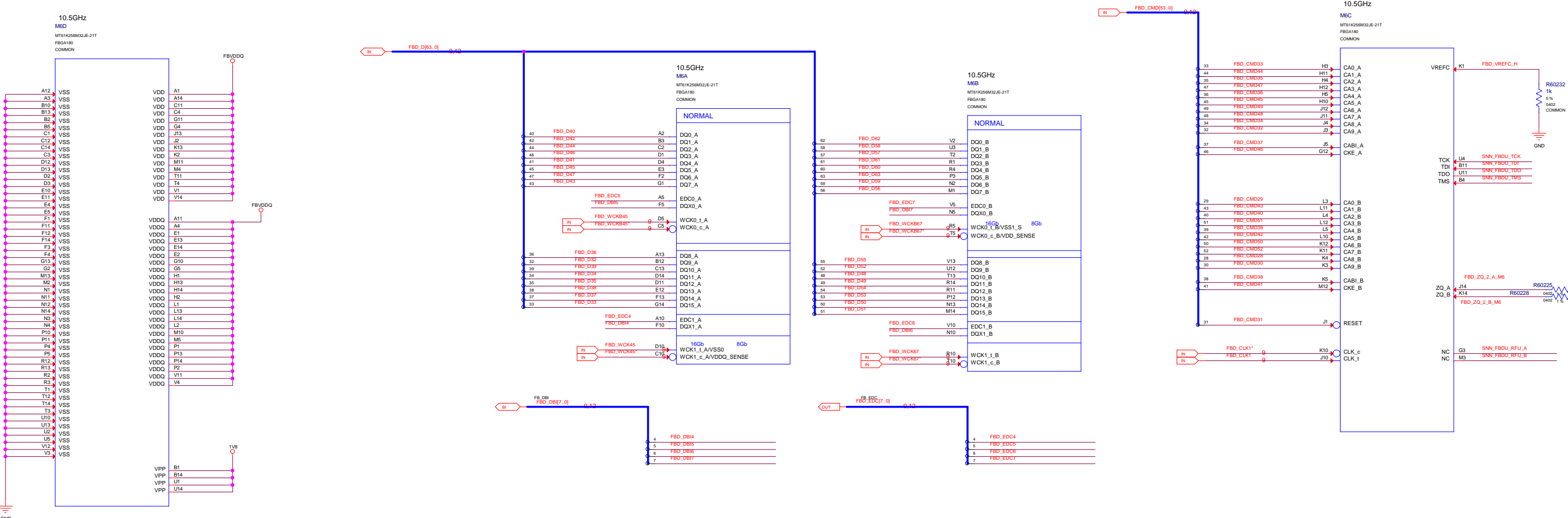
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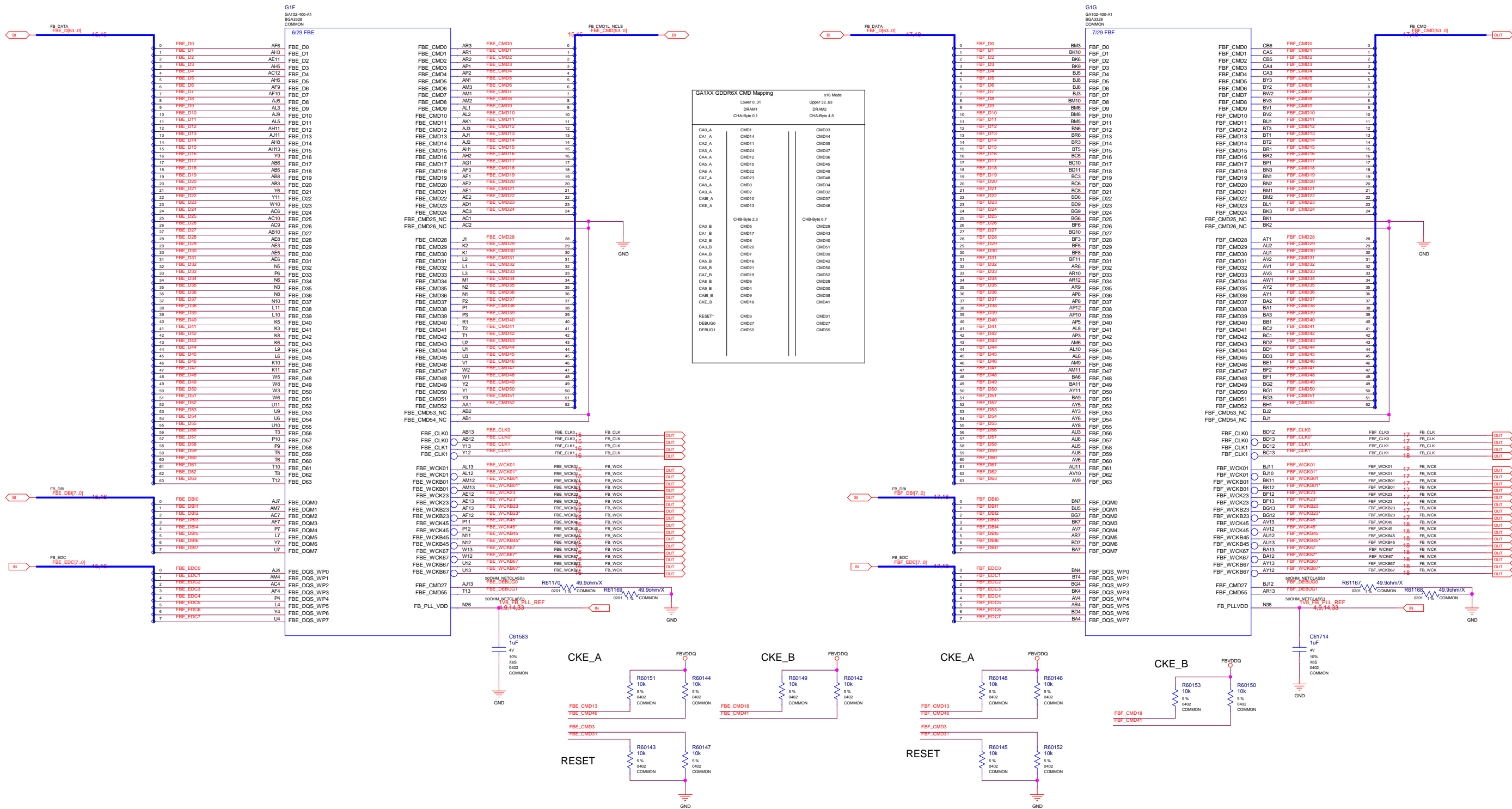
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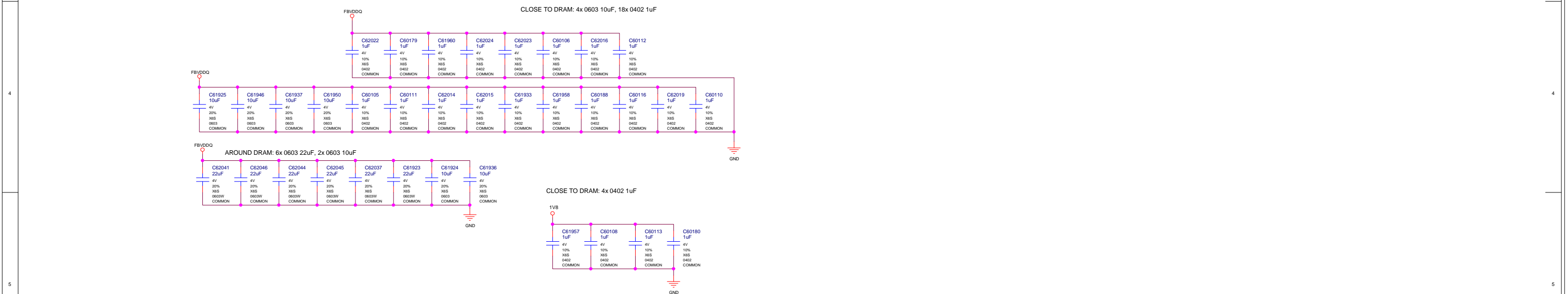
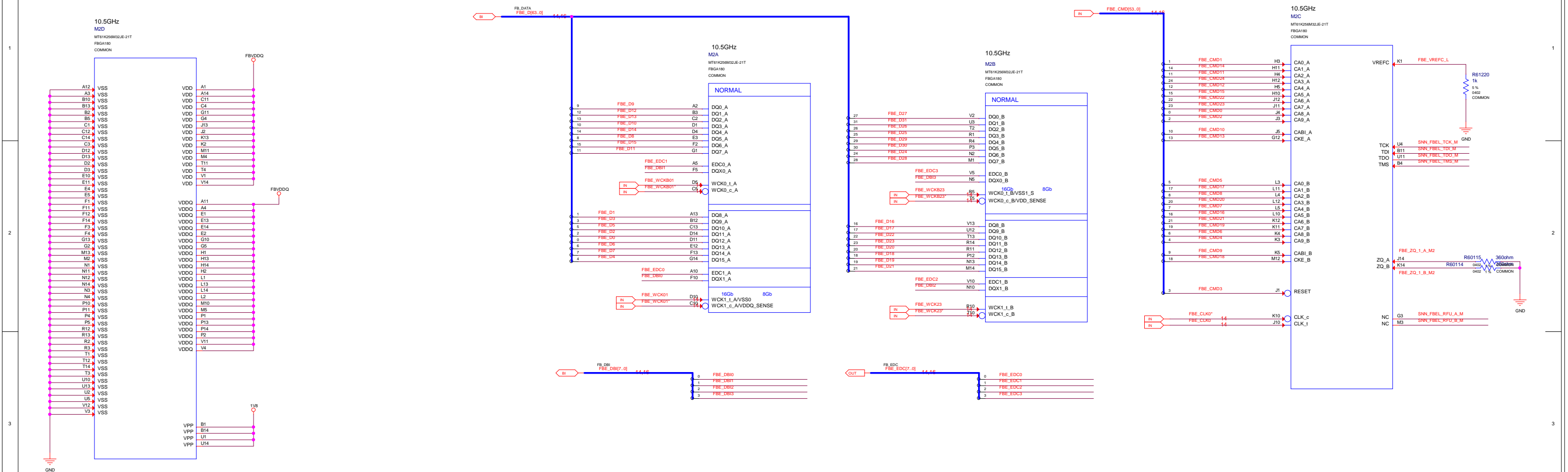


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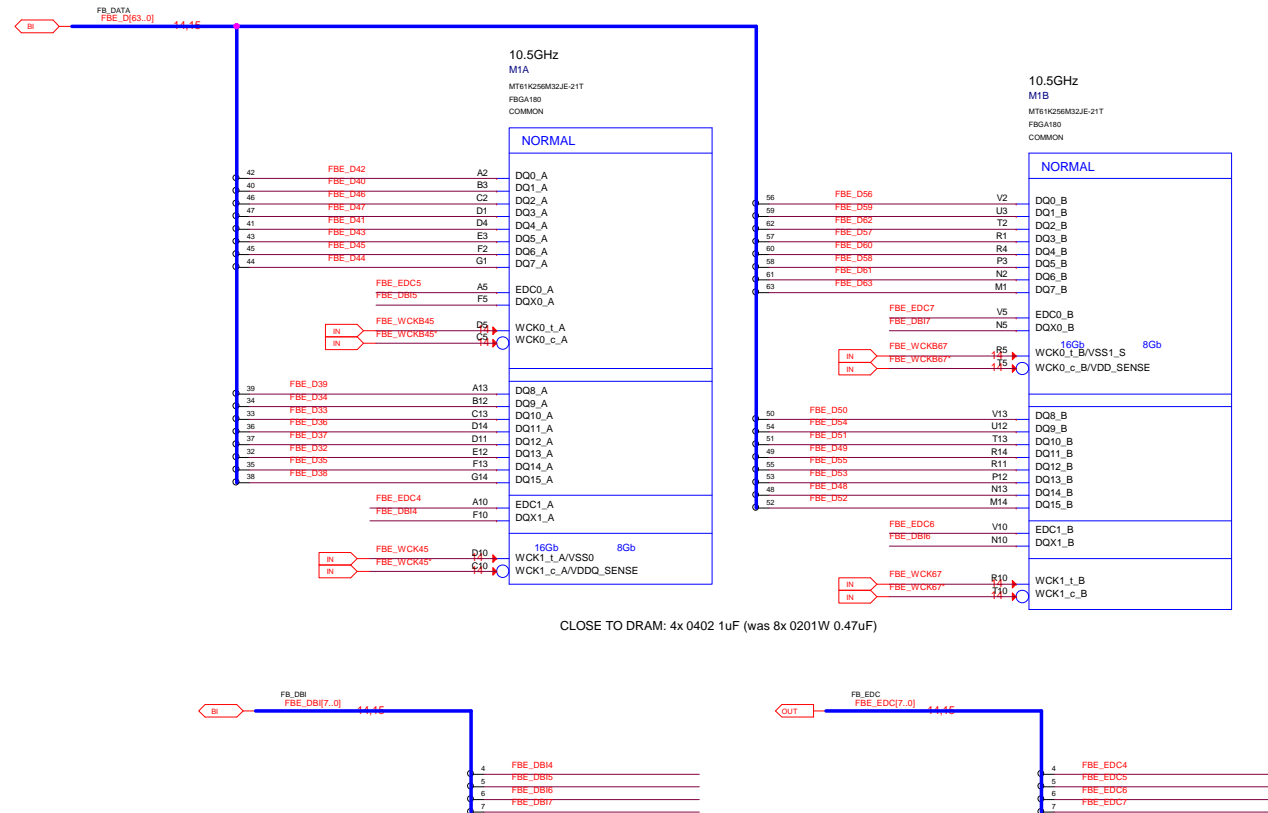
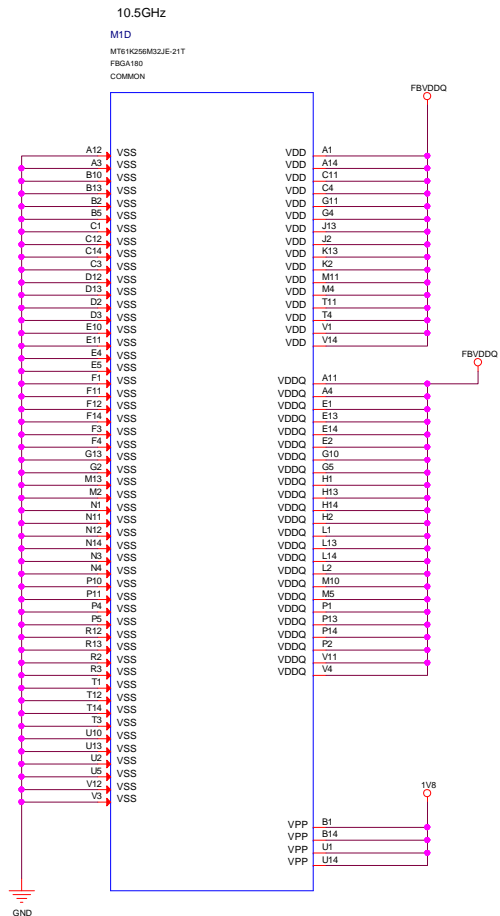


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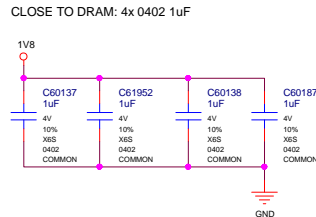
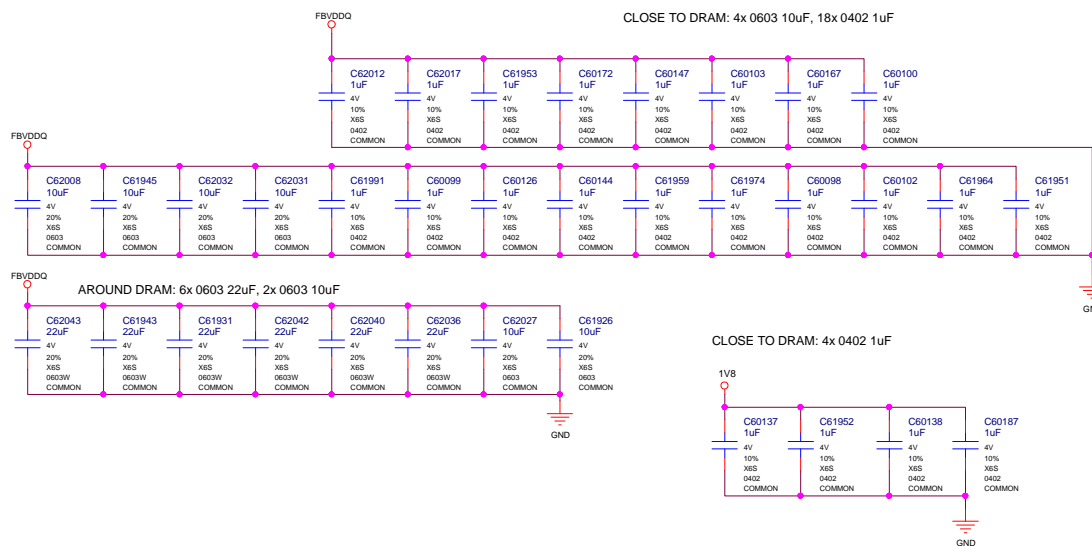




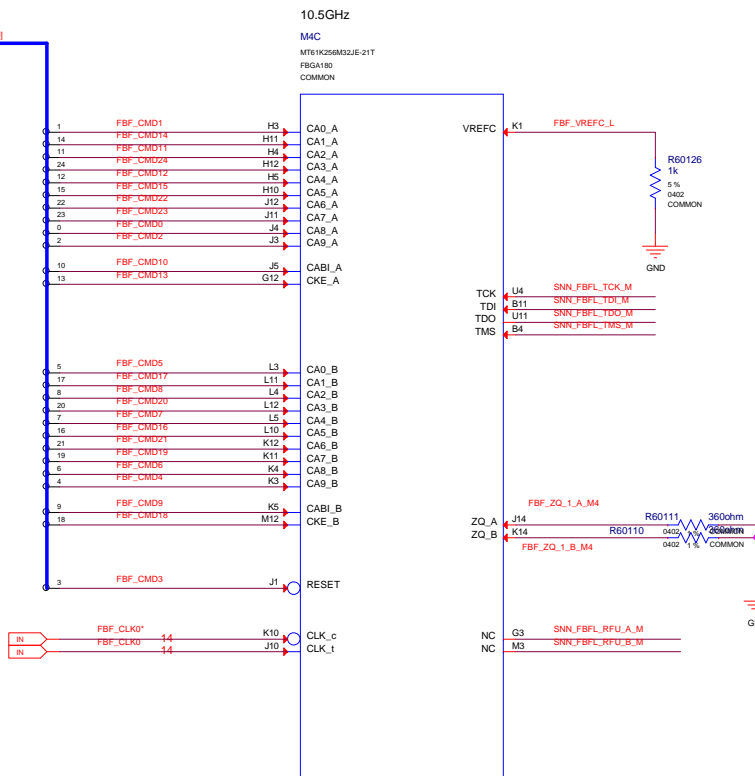
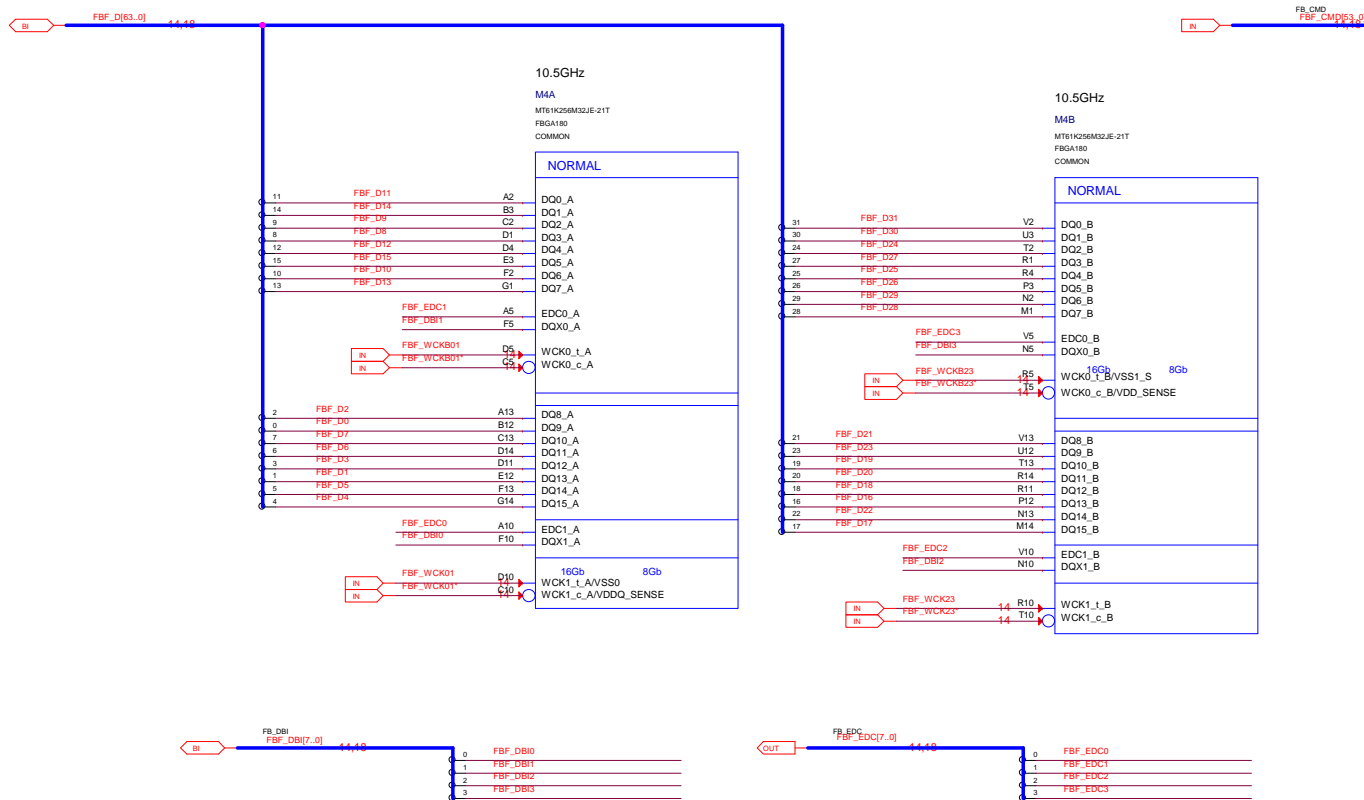
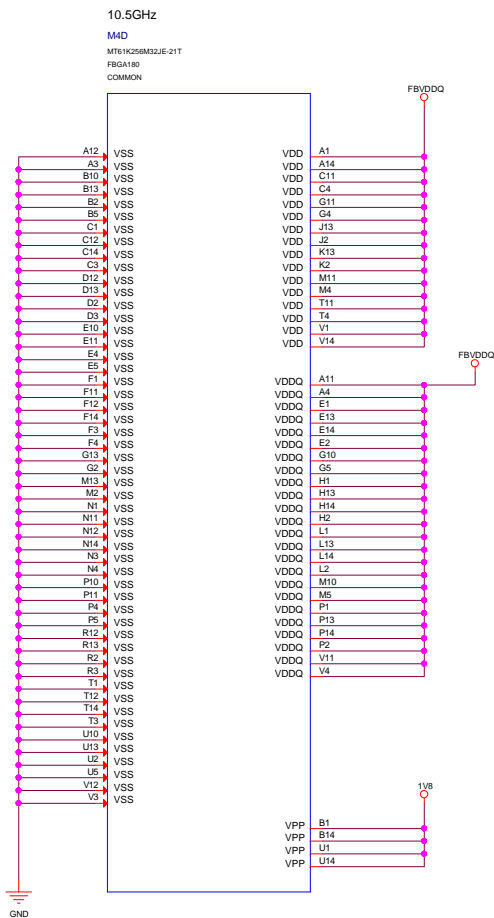
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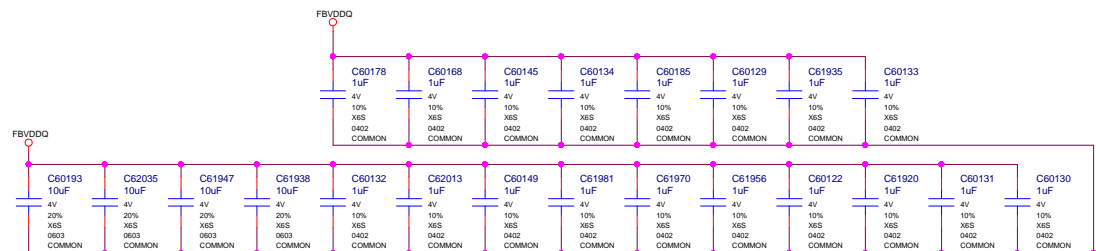
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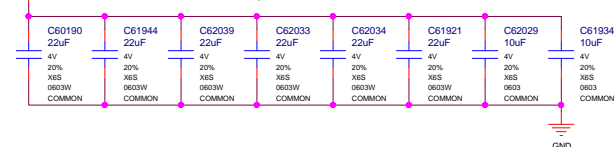
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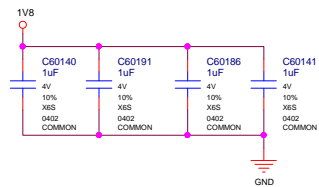
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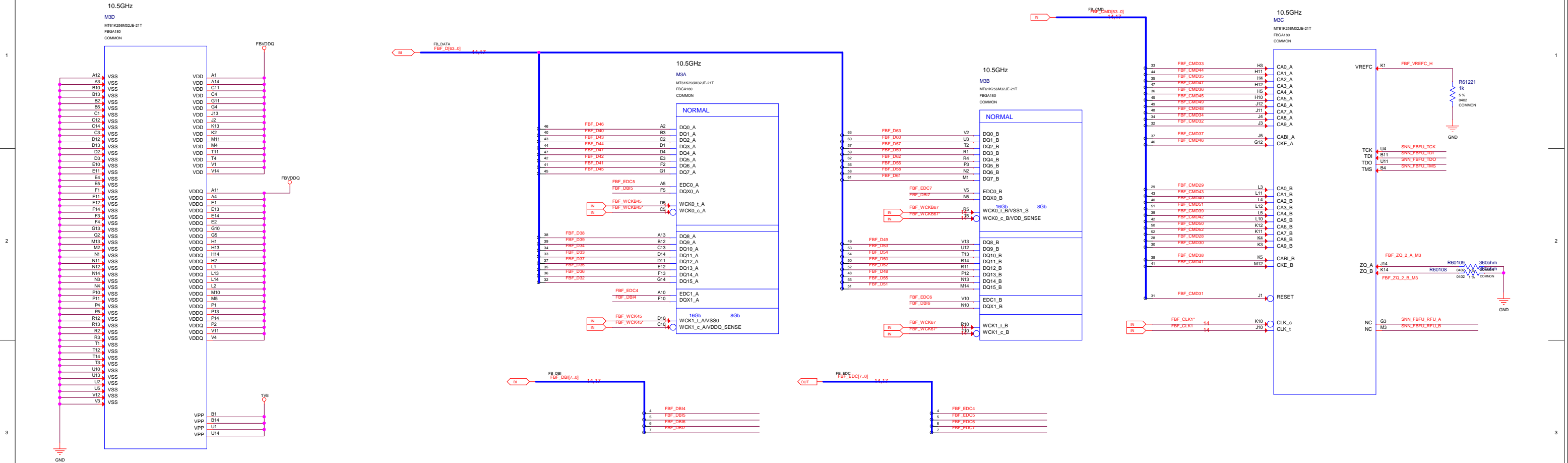
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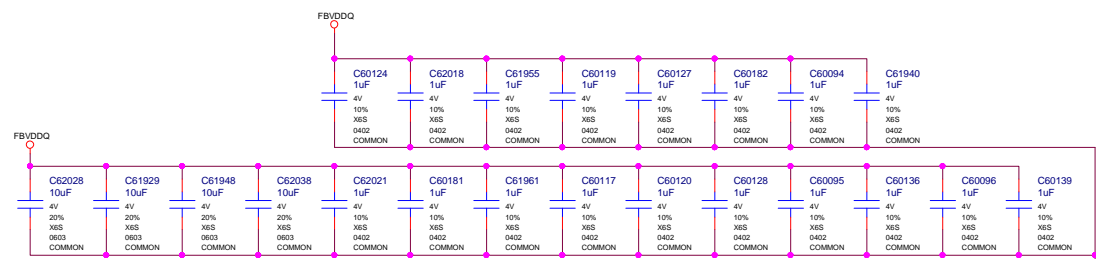
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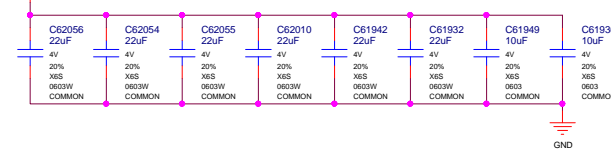
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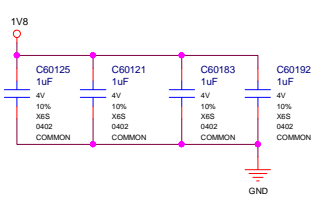
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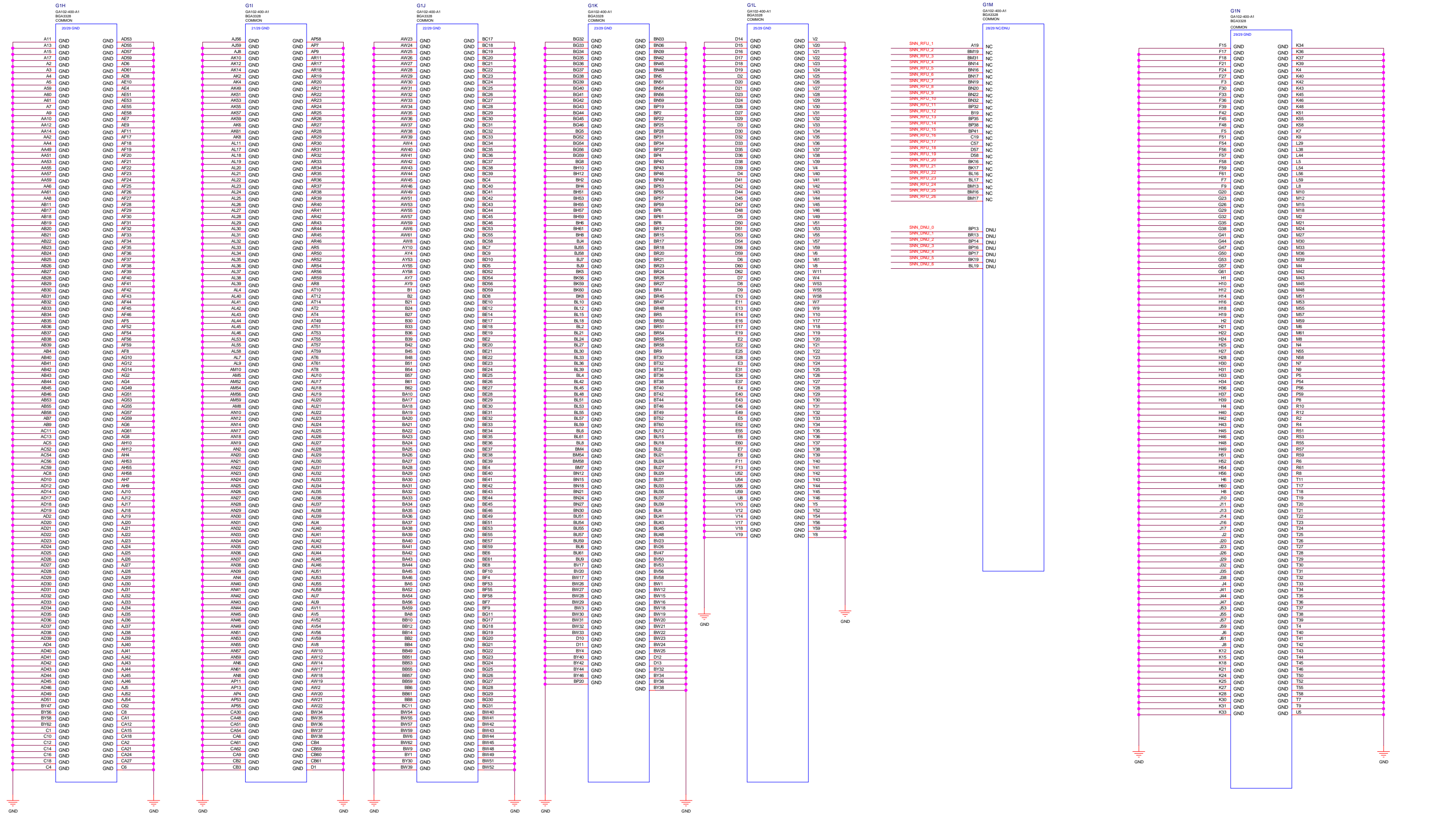


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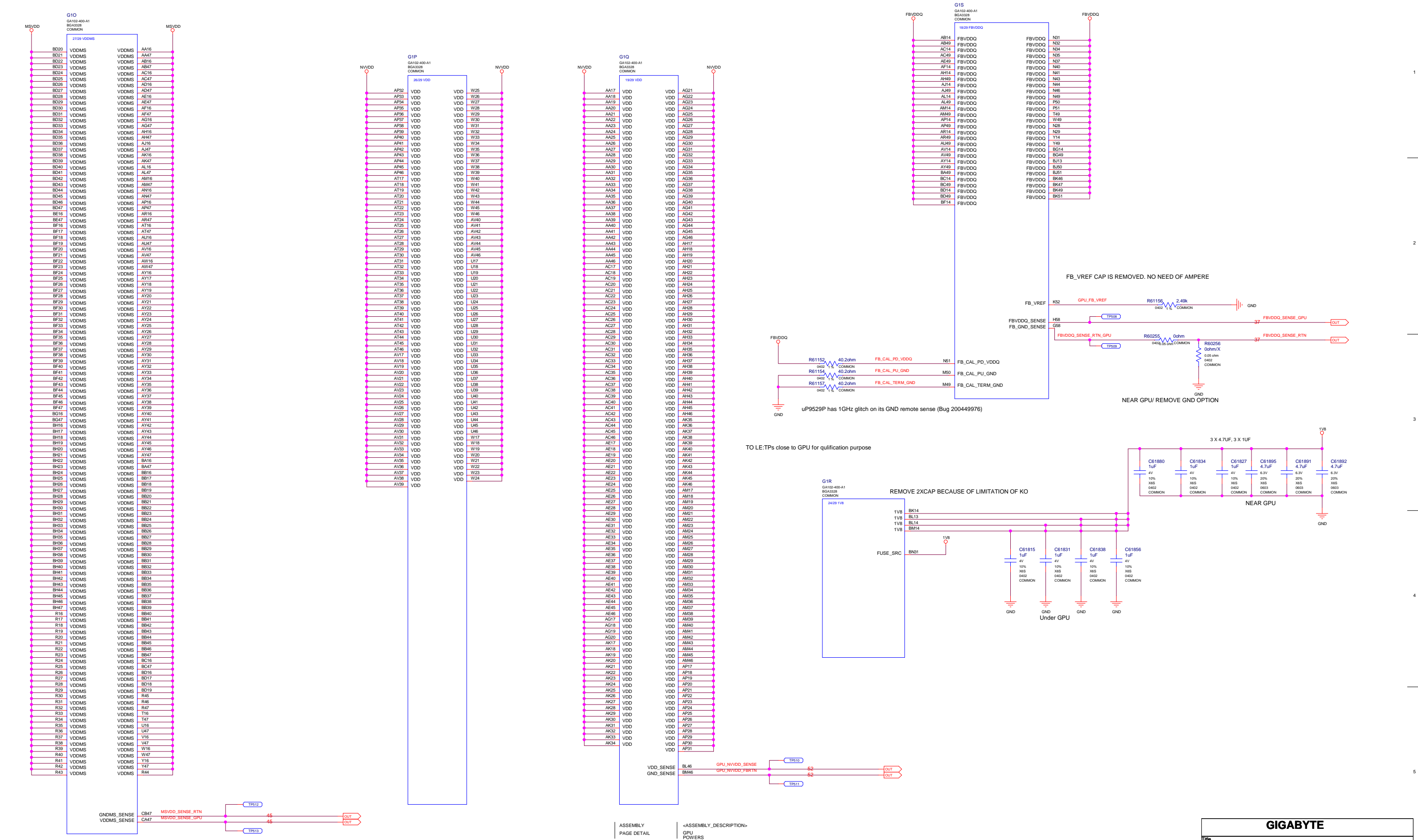
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## GPU GND, RFUs & RSVD



GPU PWR and GND



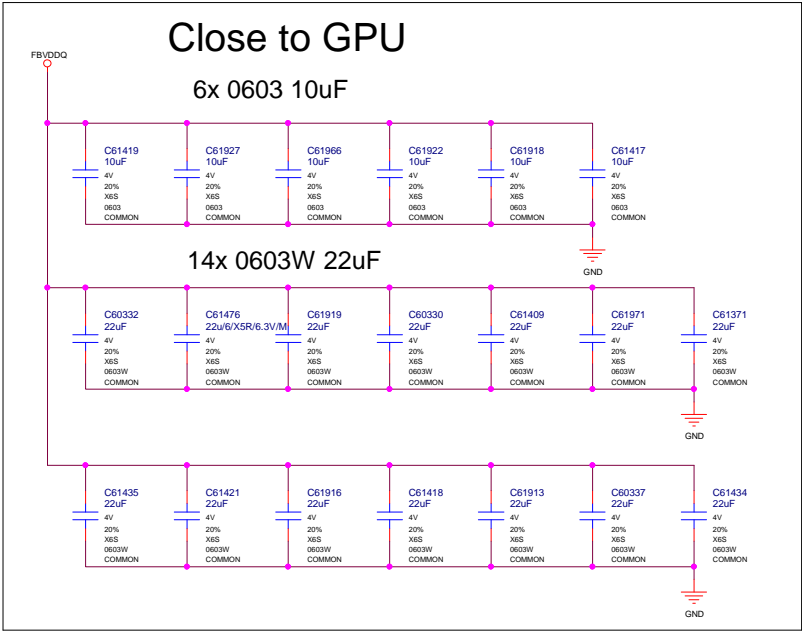
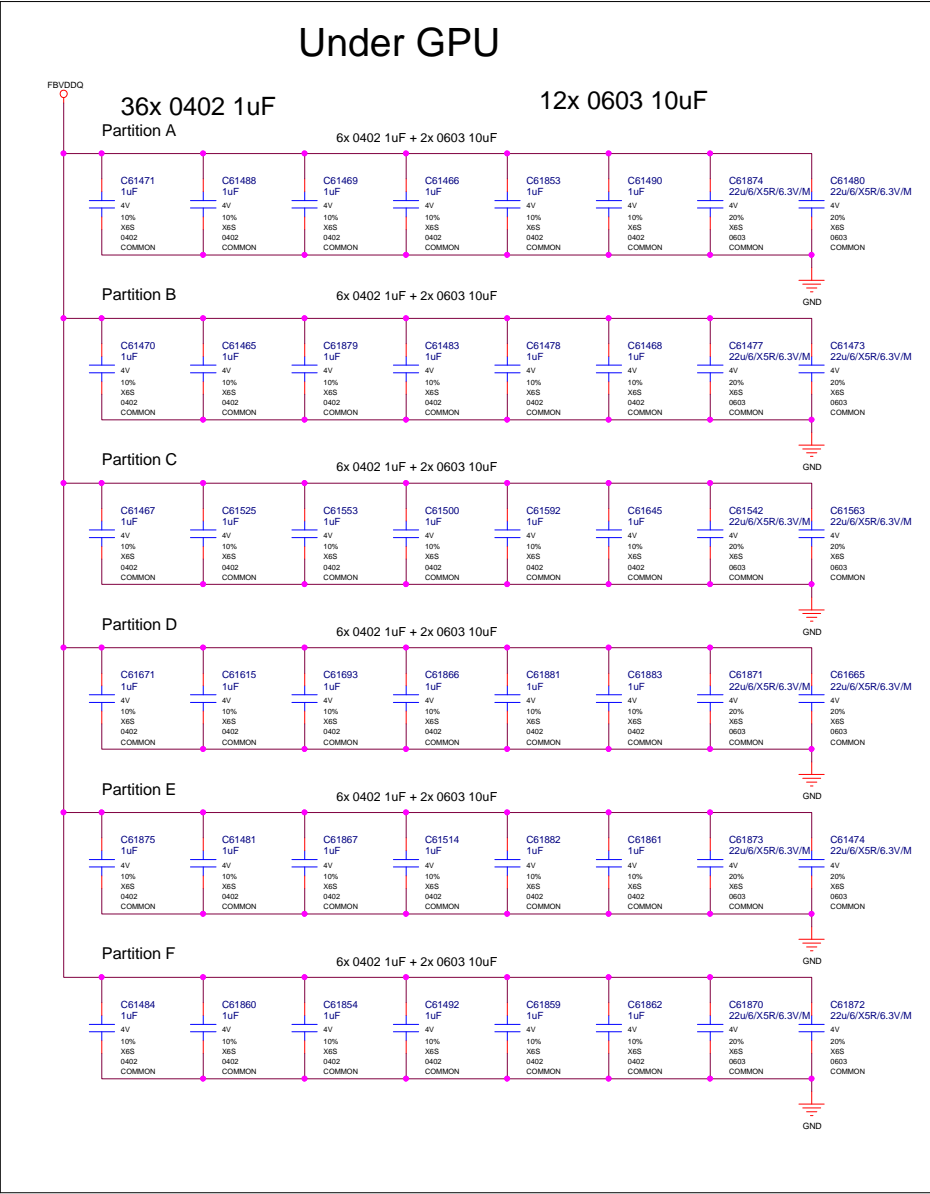
NVVDD

UNDER GPU





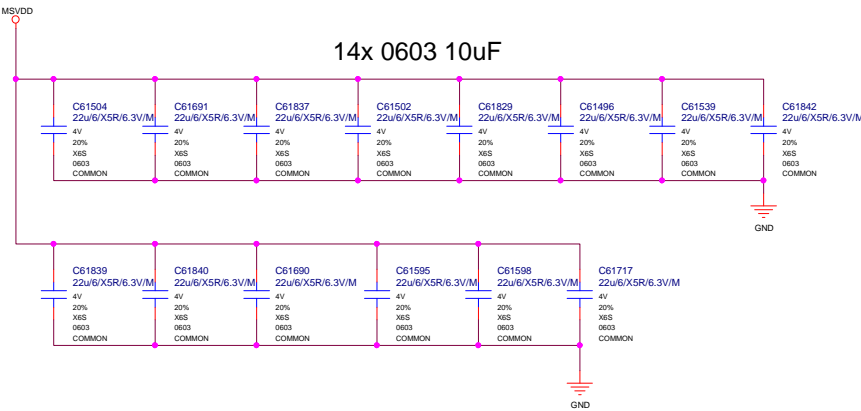
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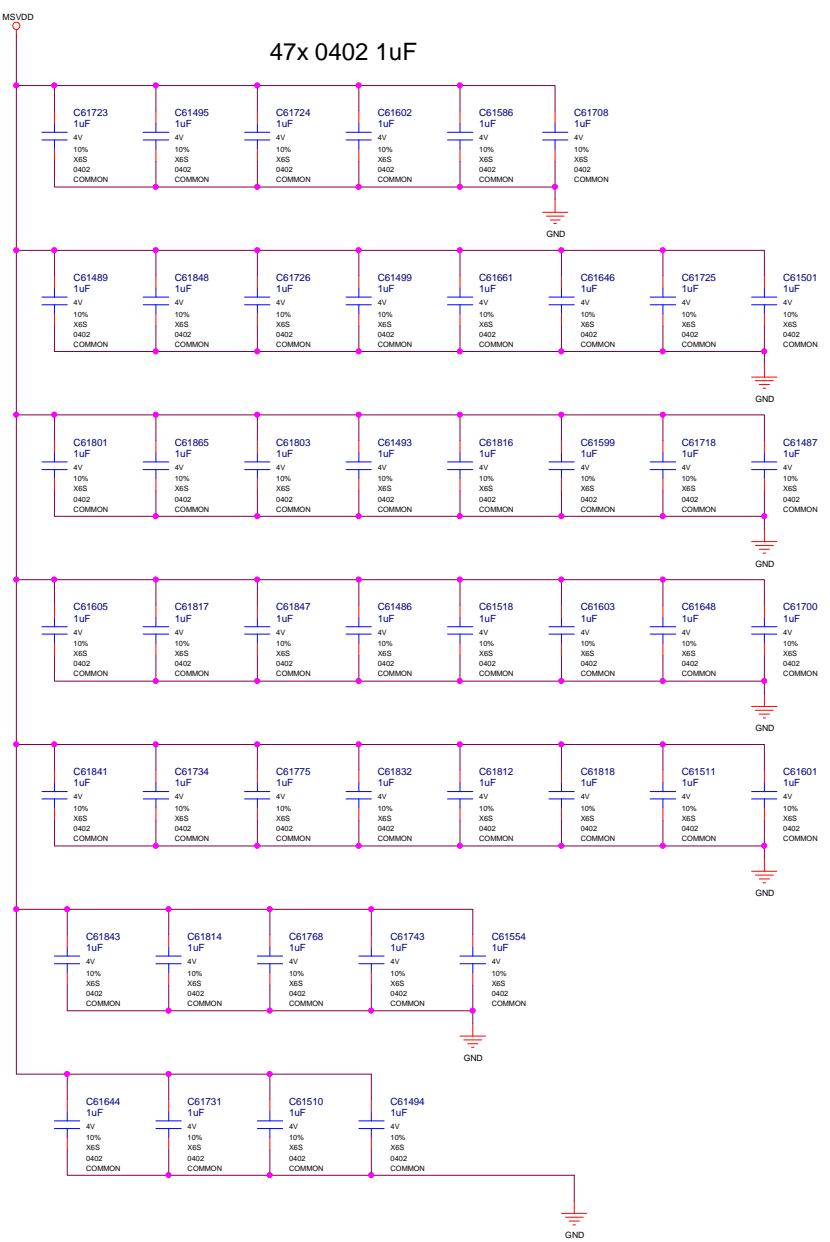
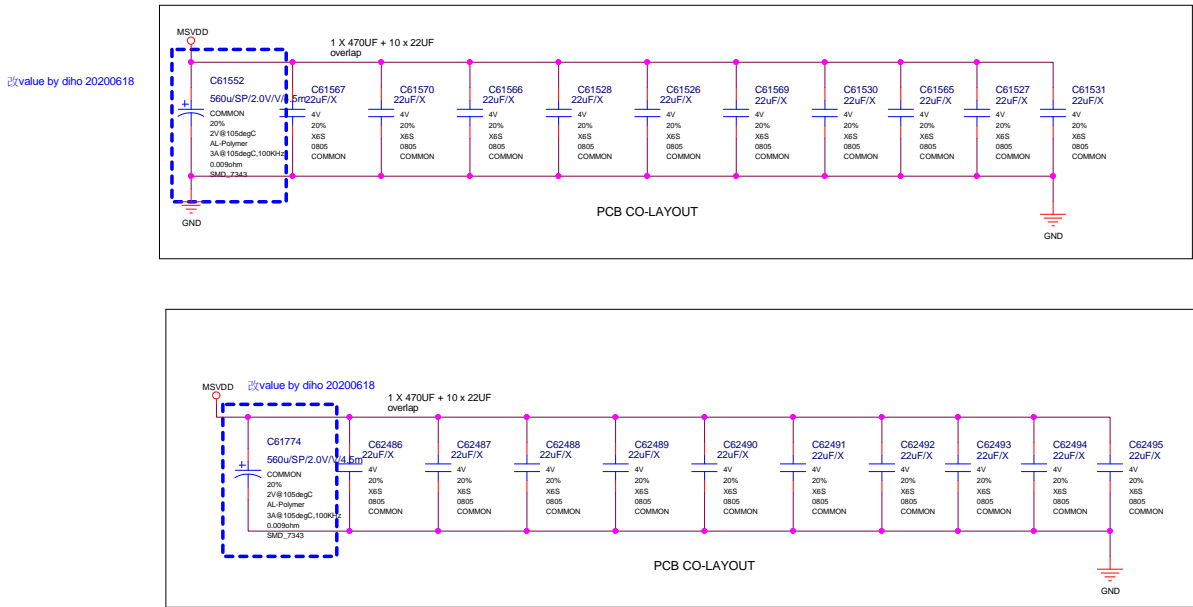


MSVDD

UNDER GPU



2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



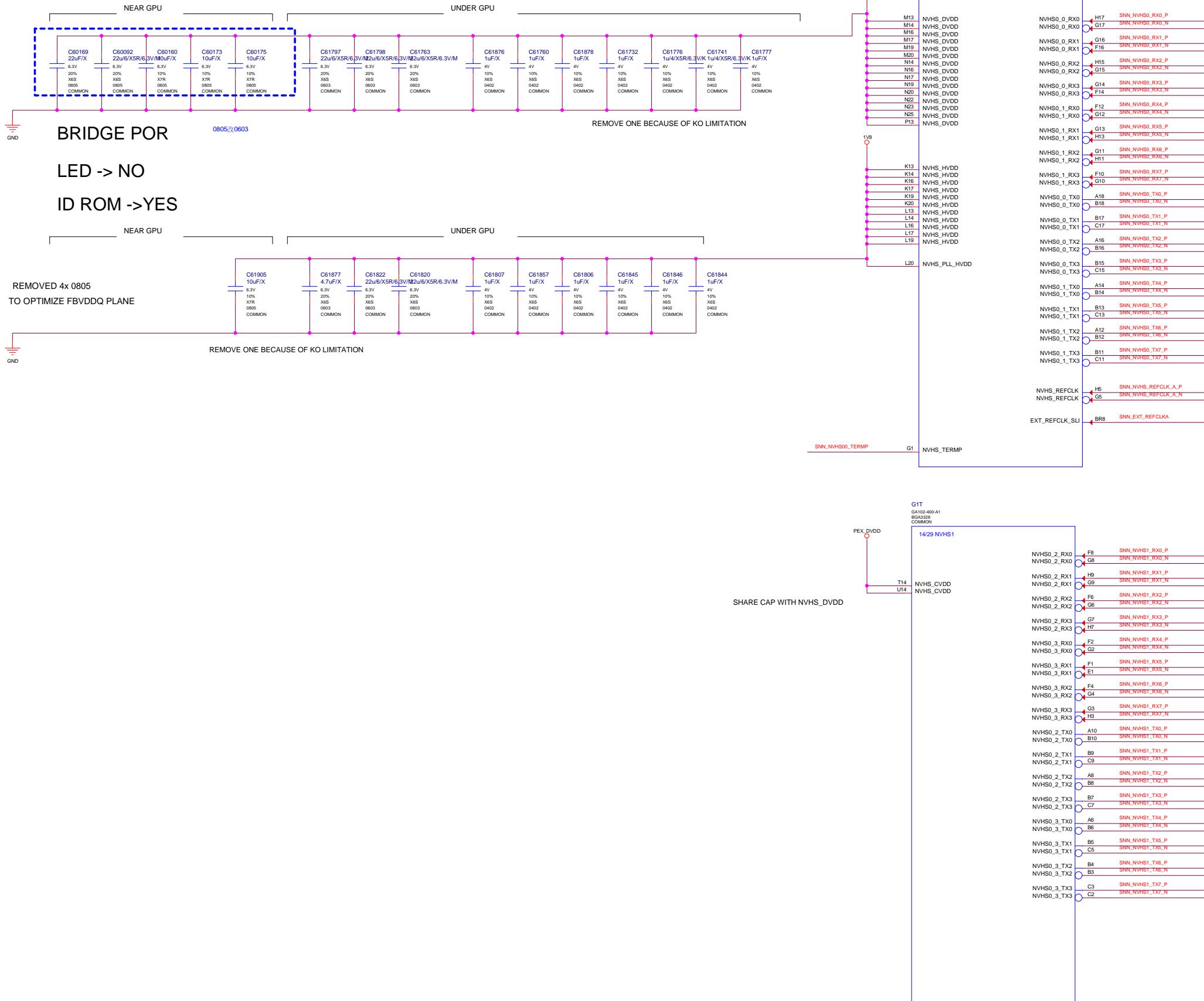
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# NVHS Interface and FRAME LOCK



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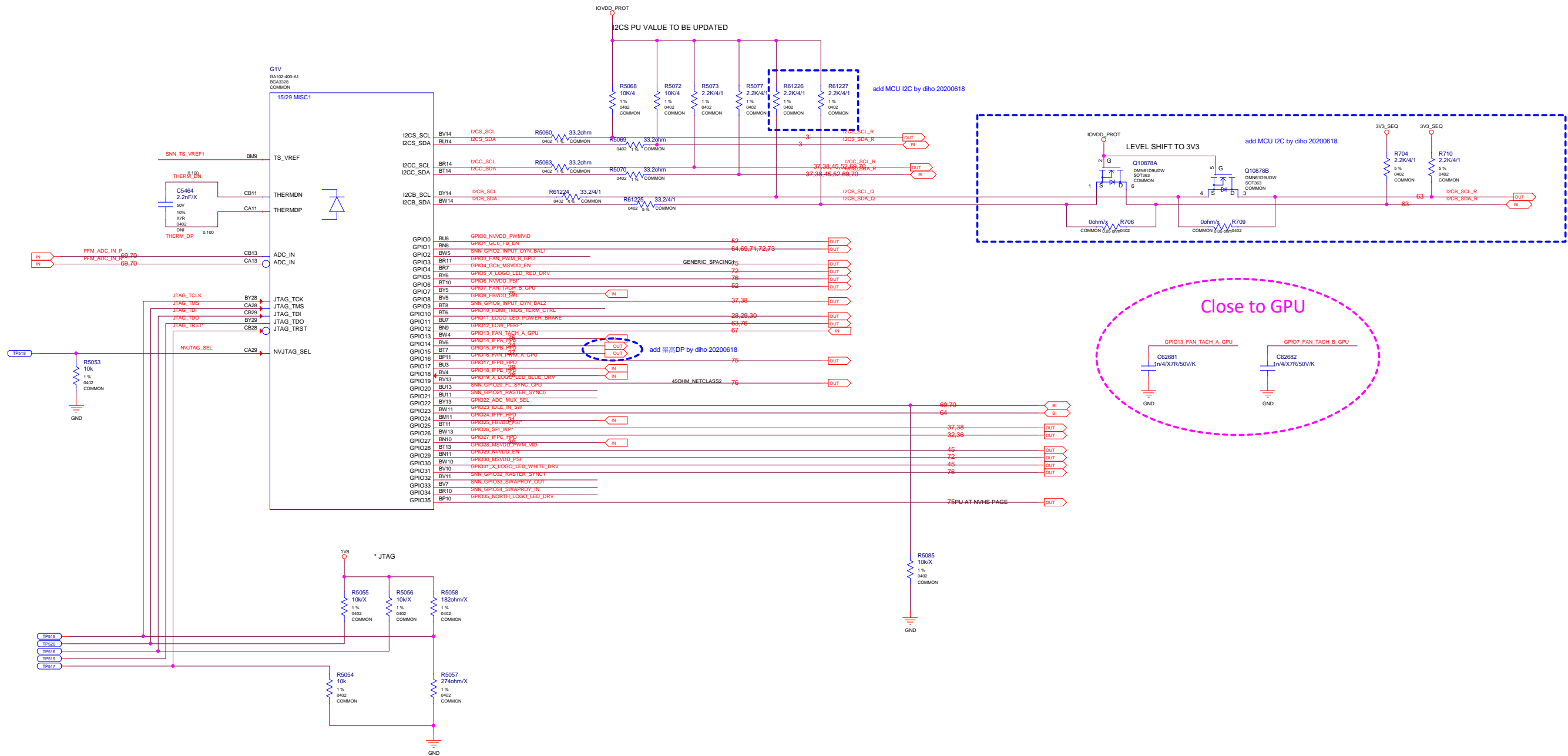
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GIGABYTE

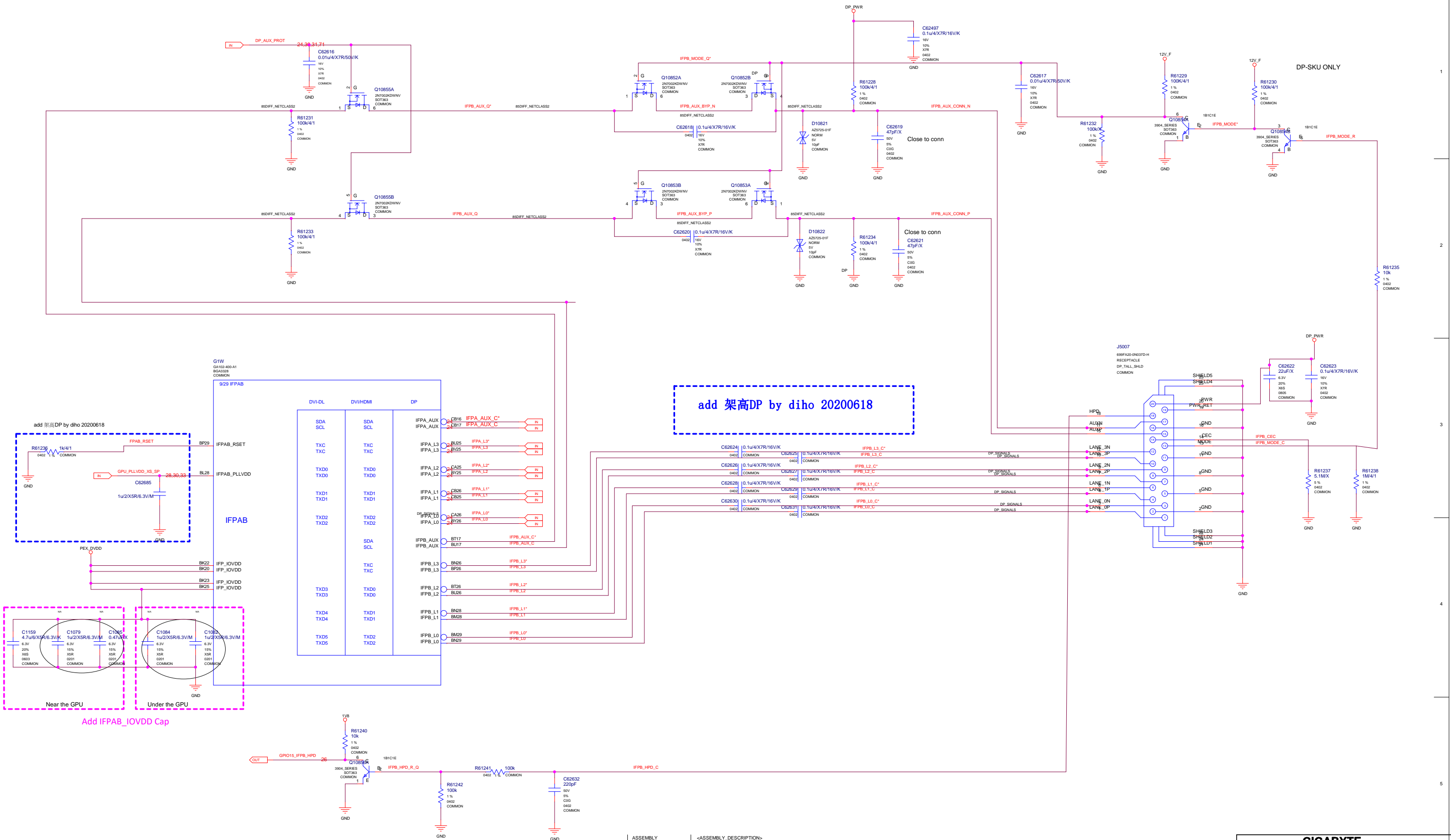
NVHS Interface and FRAME LOCK		
Title	NVHS Interface and FRAME LOCK	
Size	Document Number	Rev
Custom	GV-N3080AORUS X-10GD	1.0
Date: Monday, September 28, 2020 Sheet 25 of 80		

MISC1: Fan, Thermal, JTAG, GPIO, STEREO



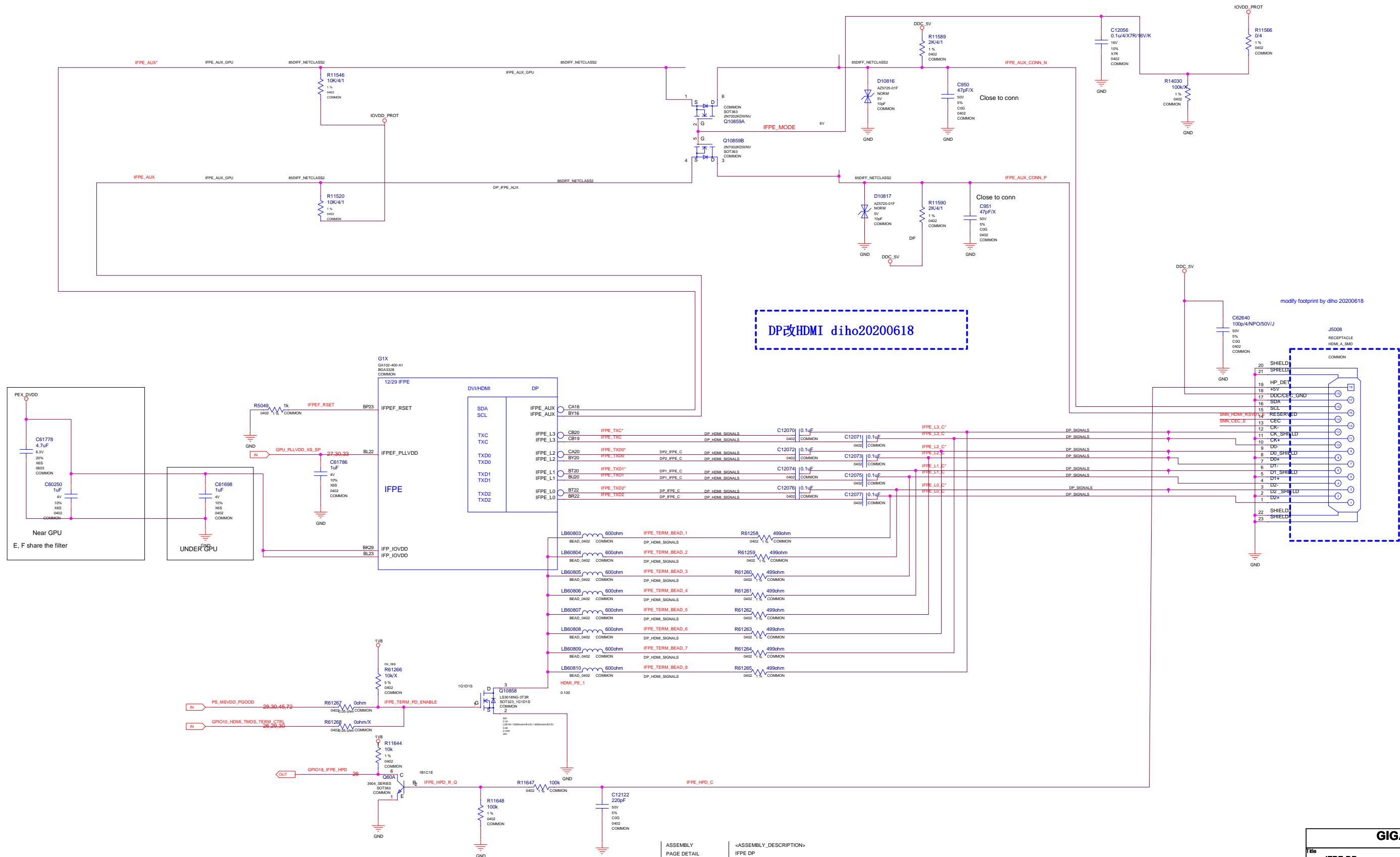
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IFPA UNUSED, IFPB UNUSED



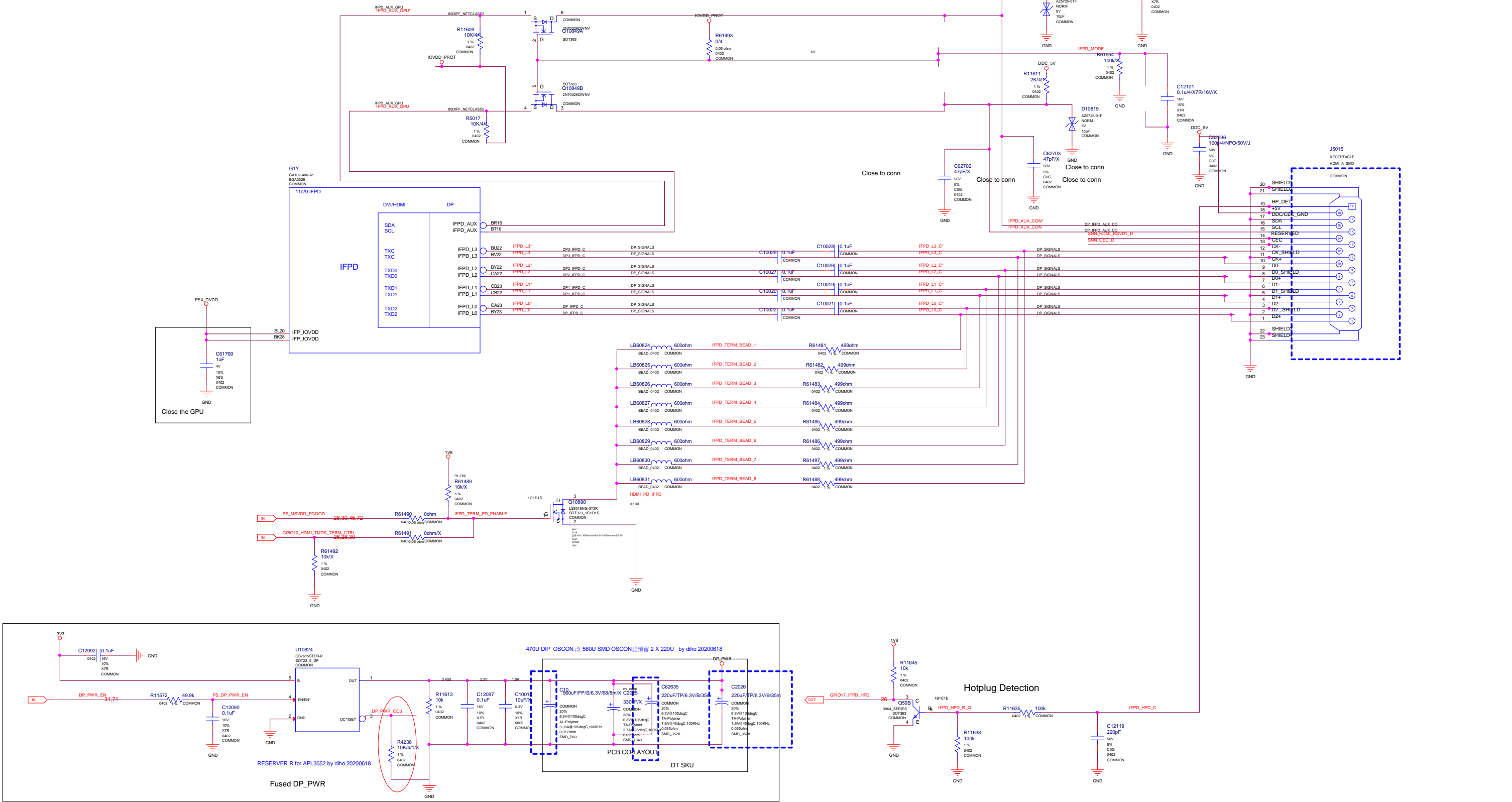
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## IFPE DP



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IFPD DP



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IFPD DP

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IFPC HDMI/DP

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4

5

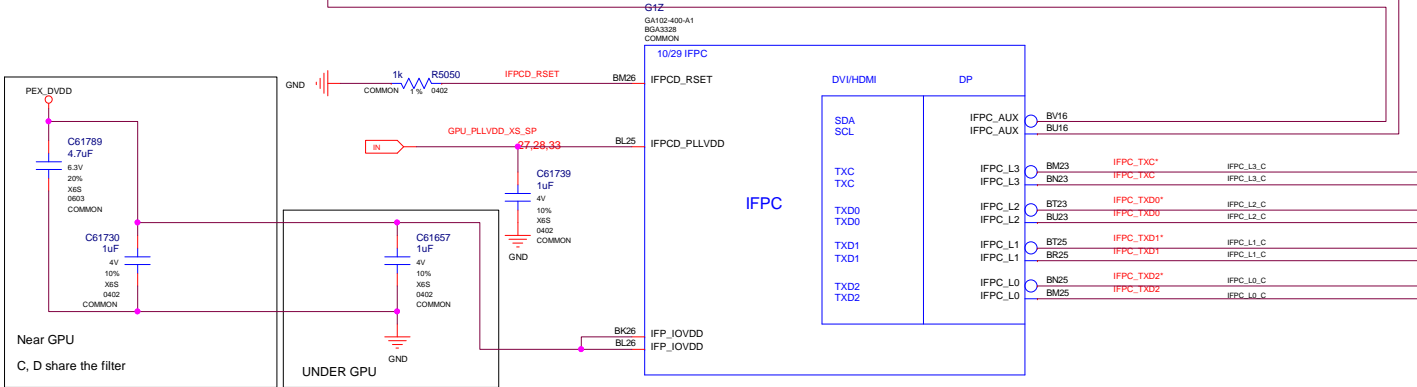
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2

3

4

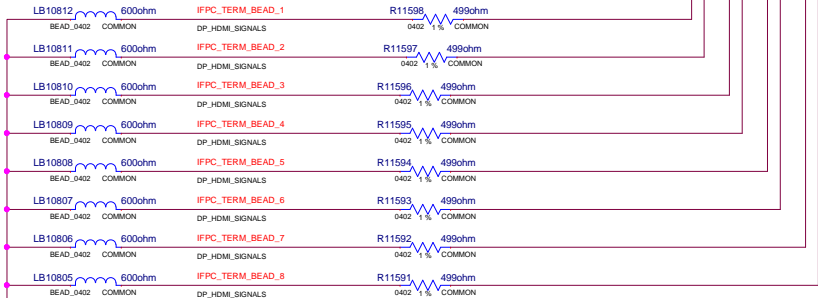
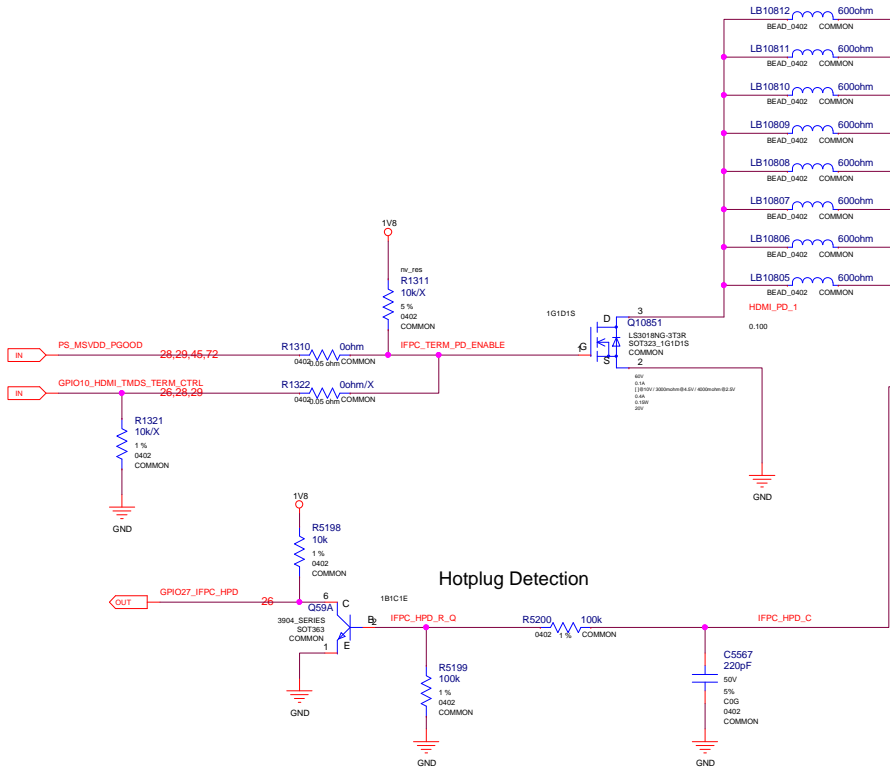
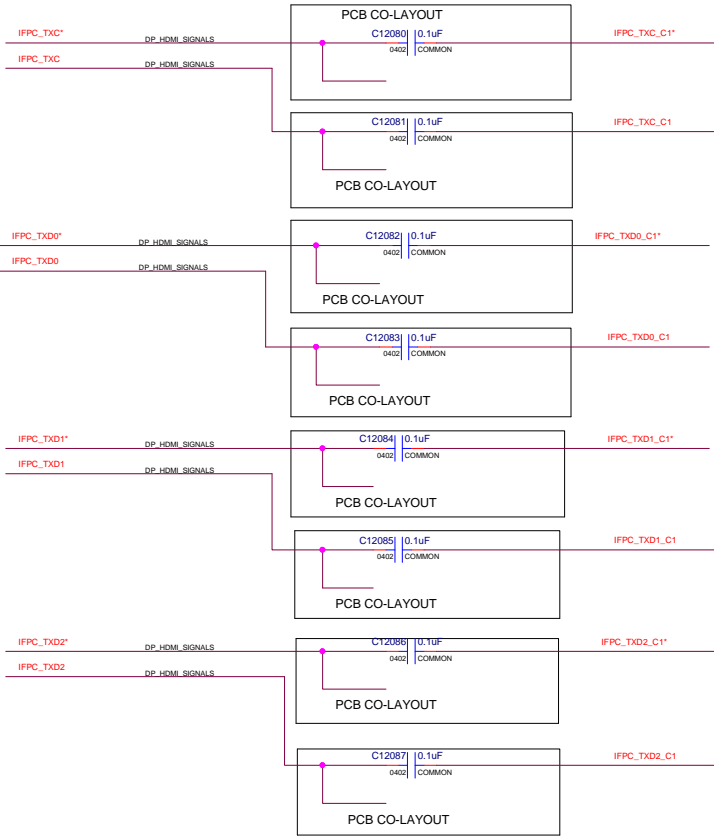
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DEL COLAY DP by diho 20200618

modify footprint by diho 20200618

DEL COLAY DP by diho 20200619



ASSEMBLY PAGE DETAIL <ASSEMBLY\_DESCRIPTION> IFPC HDMI/DP

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MISC: ROM, Straps

GROUP0				
STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)
H	L	L	00100	RAMCFG MICRON 8Gb G6X 19Gbps x8 (161-0430-900)
H	L	H	00101	RAMCFG MICRON 8Gb G6X 21Gbps x8 (161-0431-900)
L	L	M	01000	RAMCFG MICRON 8Gb G6X 20Gbps x16 (161-0424-900)
L	L	H	00001	RAMCFG MICRON 8Gb G6X 21Gbps x16 (161-0431-900)
L	M	H	01010	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
L	L	L	0000	FS_OVERT DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

DEFAULT

Default

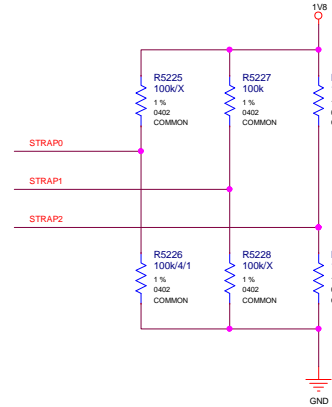
H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

<-A01 PCB

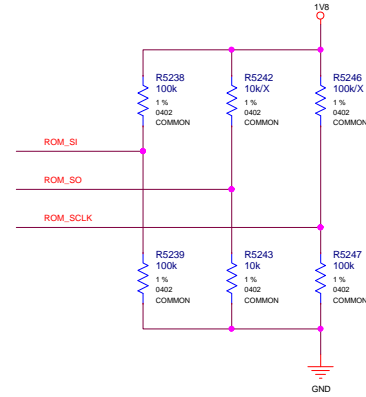
<-OLD

<-LATEST A02 PCB

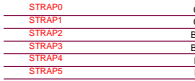
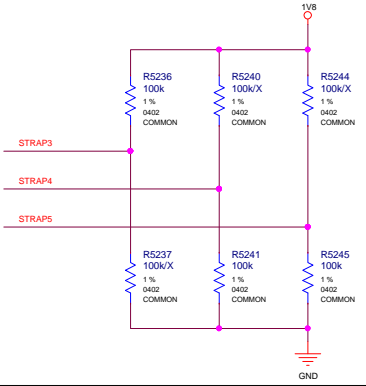
GROUP0



GROUP1



GROUP2



G1AB  
GA102-450-A1  
R5A3029  
COMMON

17/29 MISC2

ROM\_CS  
ROM\_SI  
ROM\_SO  
ROM\_SCLK

OVERT

BN13

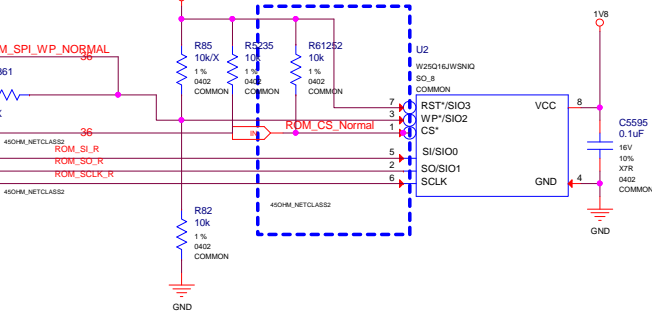
THERM\_OVERT\*

38,45,52,67,72,78

OUT



For Gaming or Server mode switch



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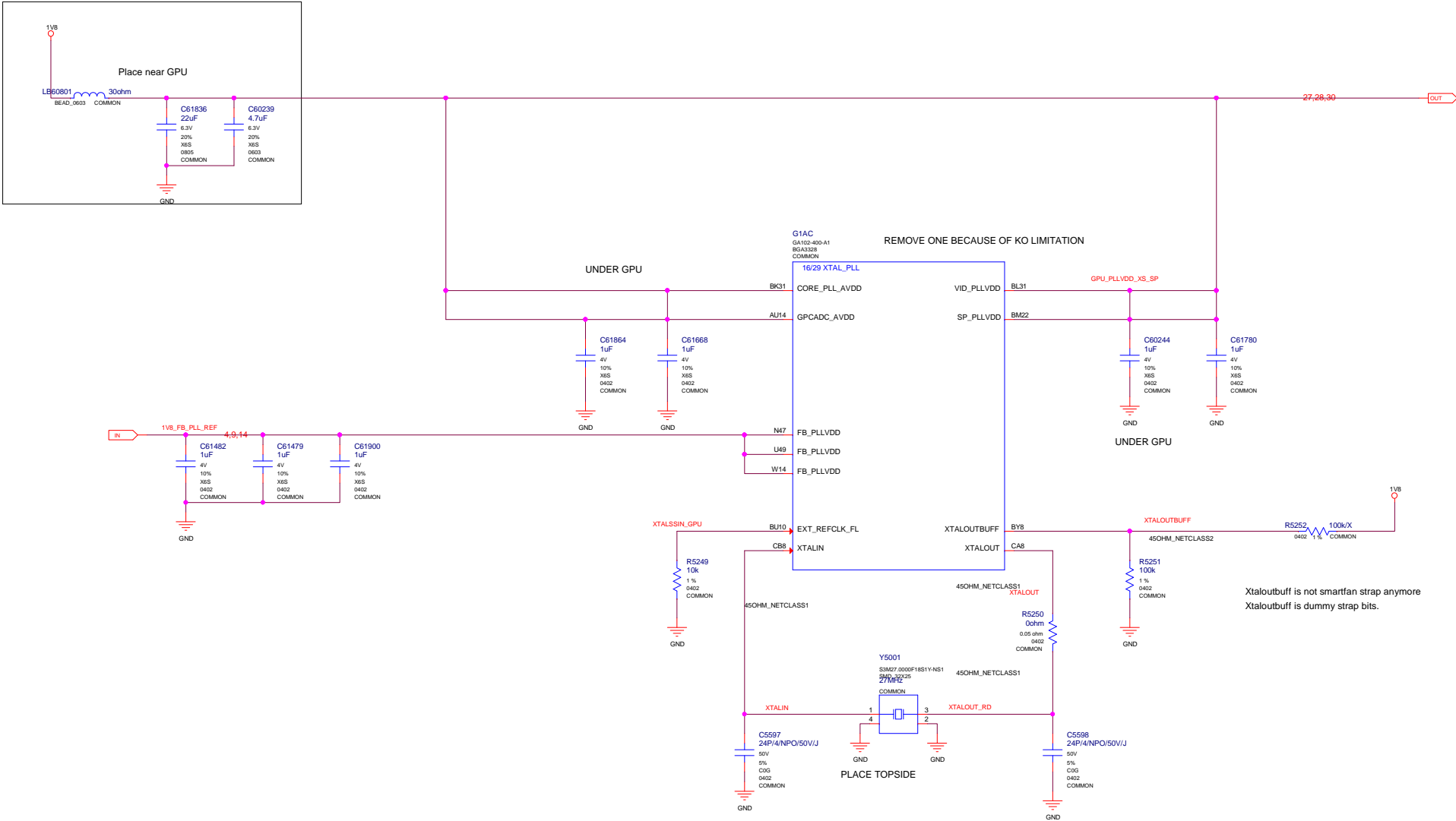
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PAGE DETAIL

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MISC. ROM, STRAPS

GIGABYTE

Title		
MISC: ROM, Straps		
Size	Document Number	H
Custom	GV-N3080AORUS X-10GD	Rev 1.0
Date:	Monday, September 28, 2020	Sheet 32 of 80

MISC: XTAL. PLL

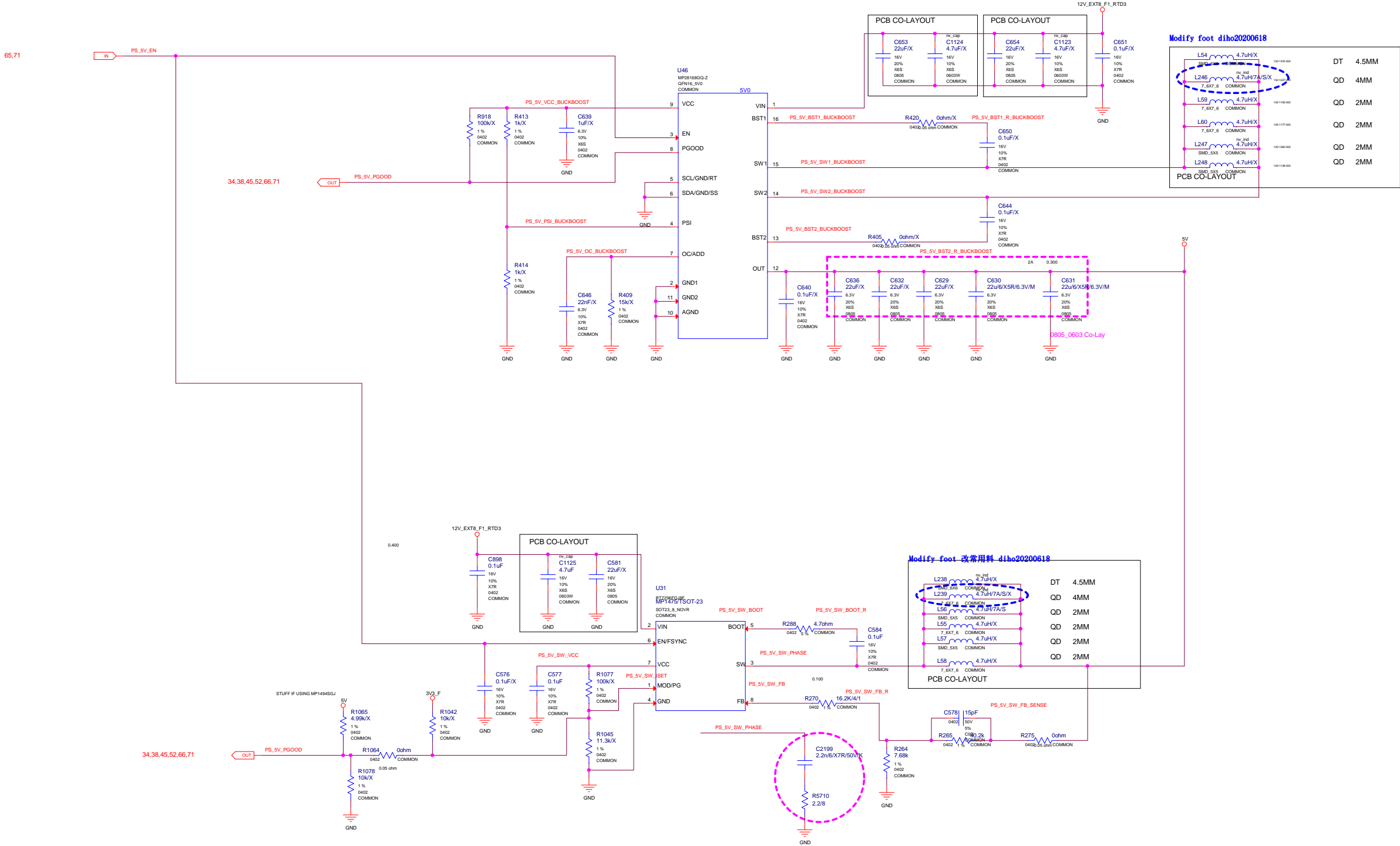


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ASSEMBLY  
PAGE DETAIL

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MISC: XTAL. PLL

PS: 5V, 5V\_BACKUP



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ASSEMBLY  
PAGE DETAIL  
<ASSEMBLY\_DESCRIPTION>  
PS: 5V

GIGABYTE			
Title PS: 5V, 5V_BACKUP			
Size Custom	Document Number GV-N3080AORUS X-10GD		Rev 1.0
Date: Monday, September 28, 2020		Sheet 34	of 80

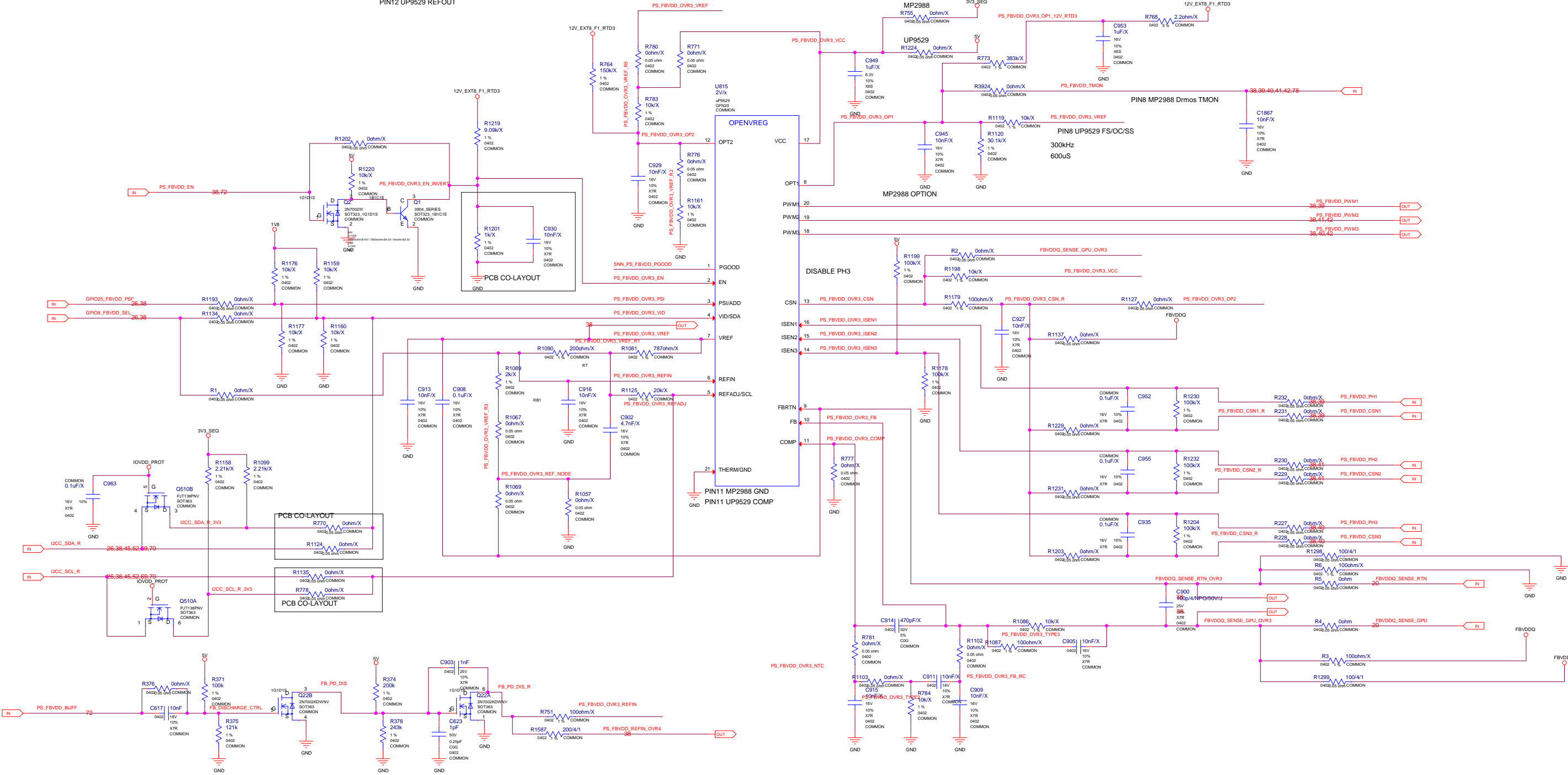






PS: FBVDD Controller OVR3

PIN12 MP2988 VIN SENSE 1/16 DIVIDER  
PIN12 UP9529 REFOUT



FOR DT SKU

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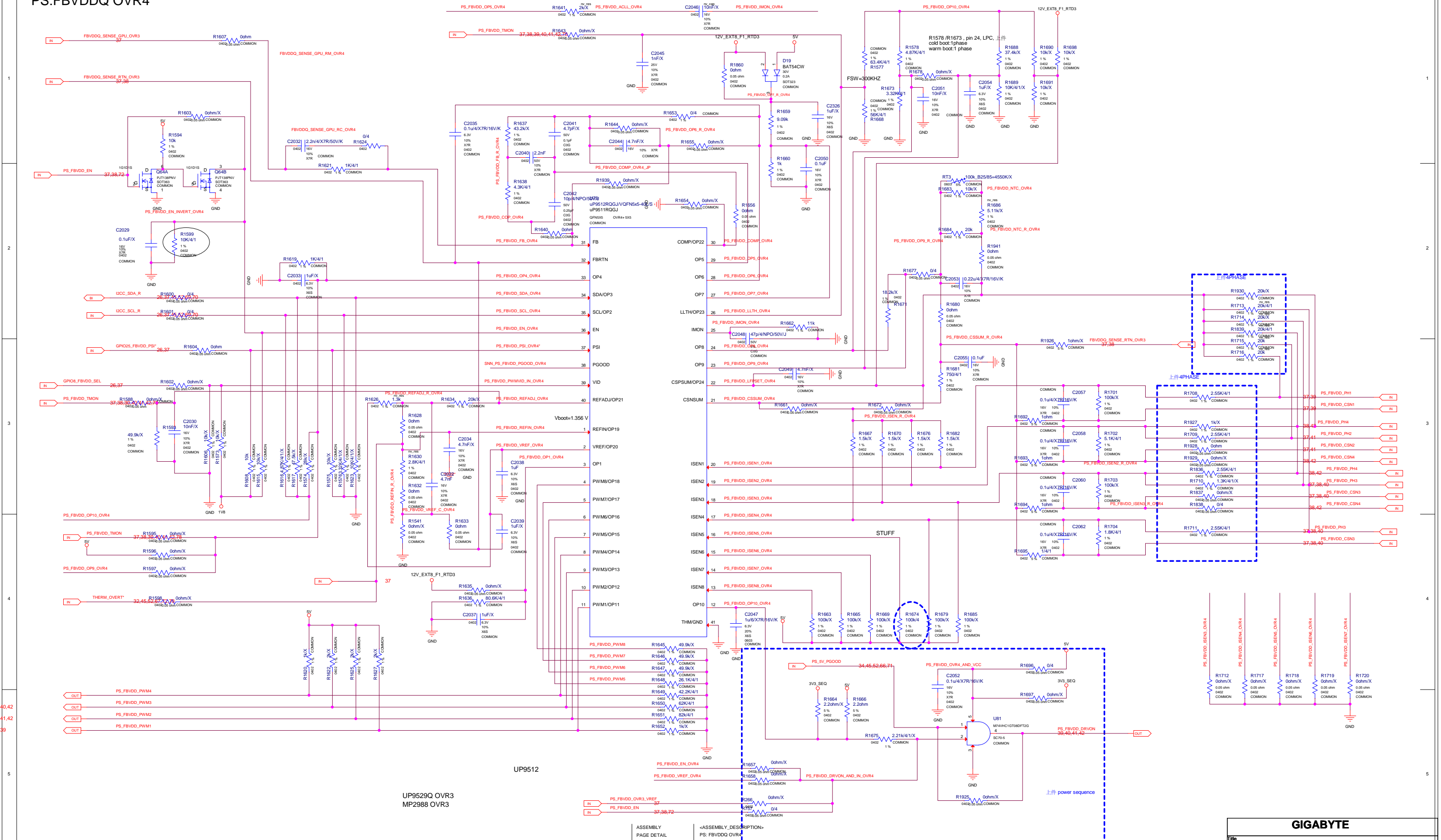
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PAGE DETAIL

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PS: FBVDD Controller OVR3

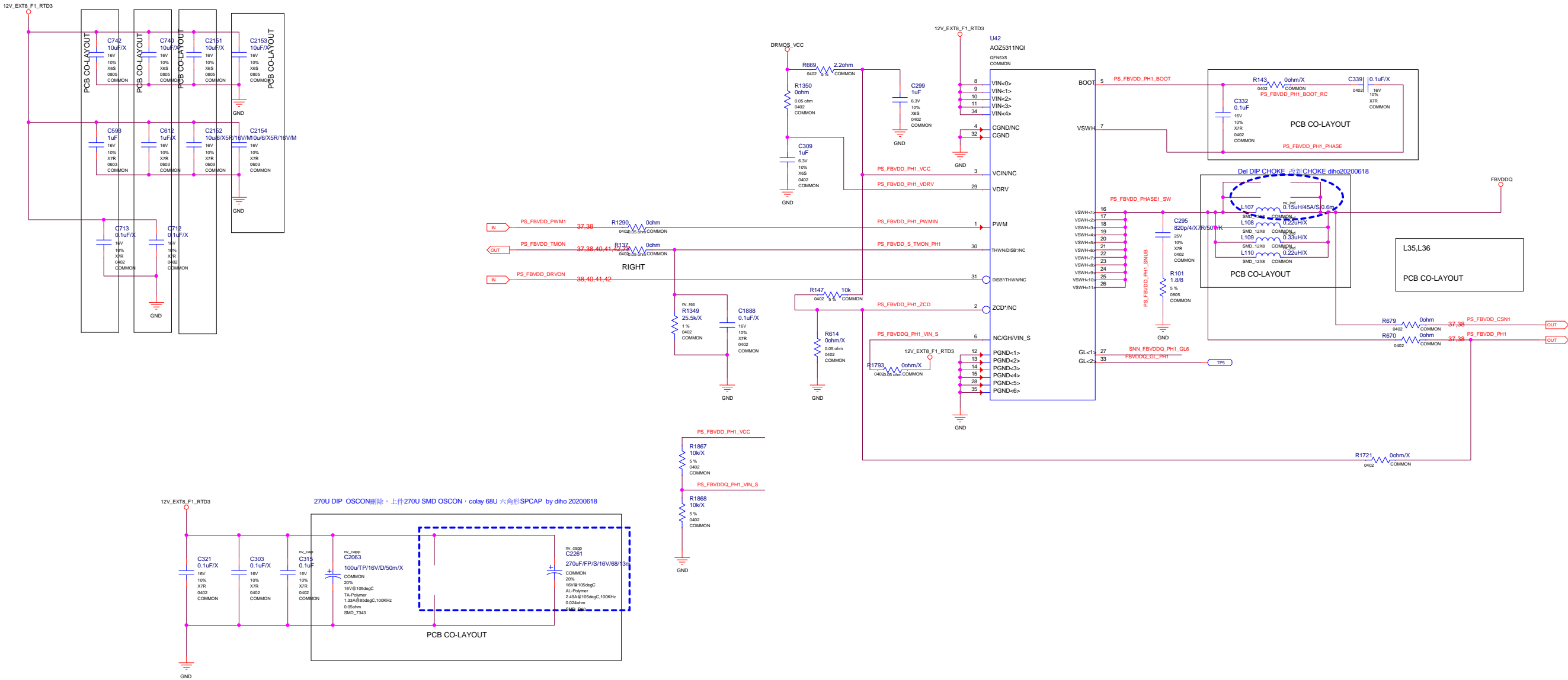
GIGABYTE

Title			PS: FBVDD Controller OVR3
Size	Custom	Document Number	GV-N3080AORUS X-10GD
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## PS:FBVDDQ OVR4



PS: FBVDD PH1



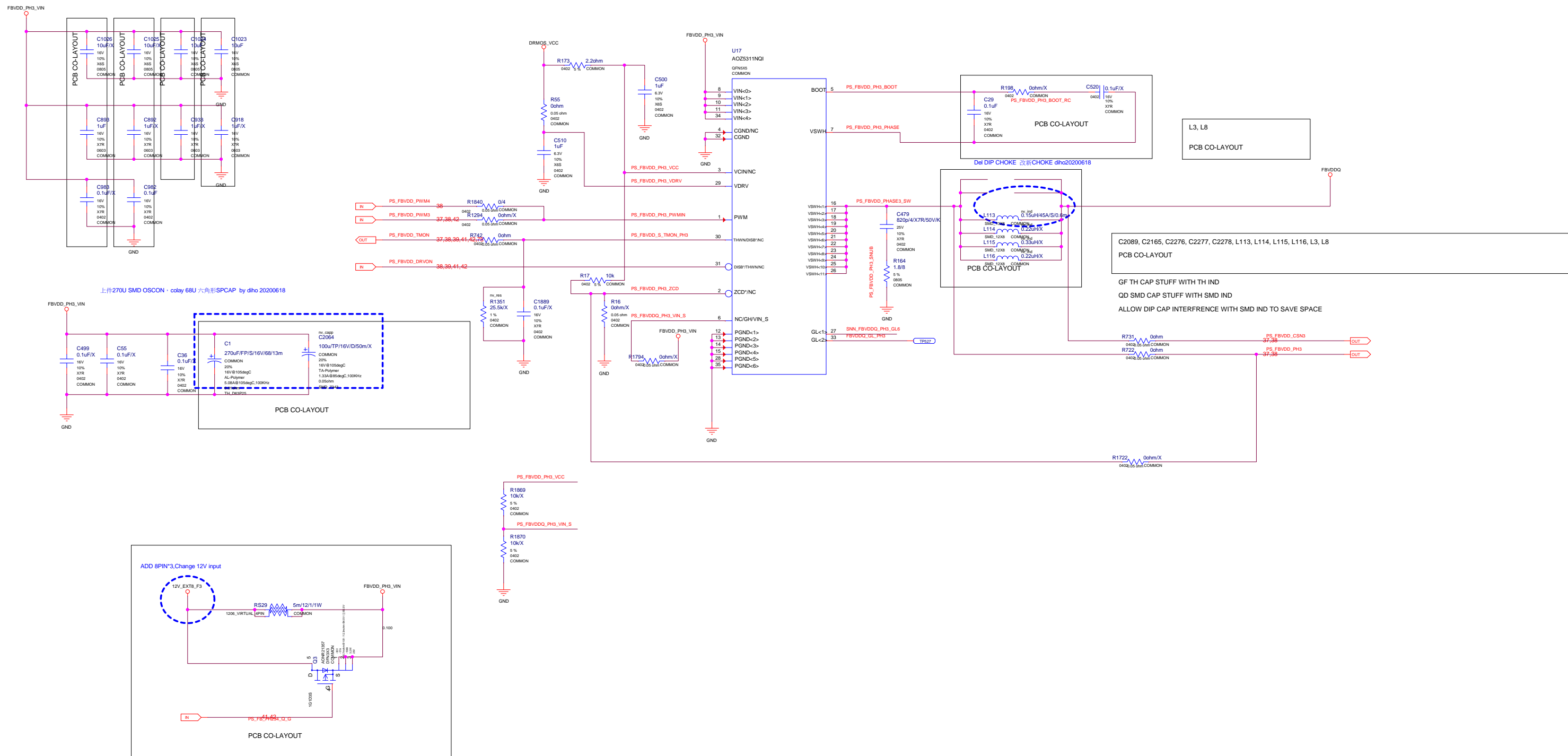
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PAGE DETAIL

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PS: FBVDD PH1

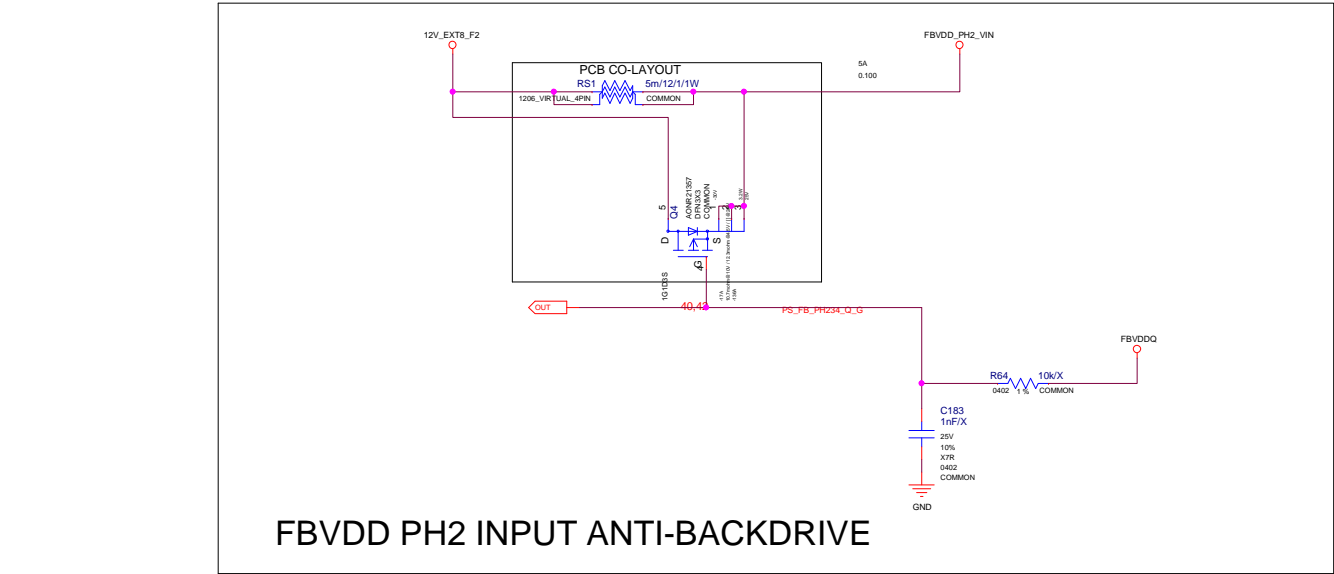
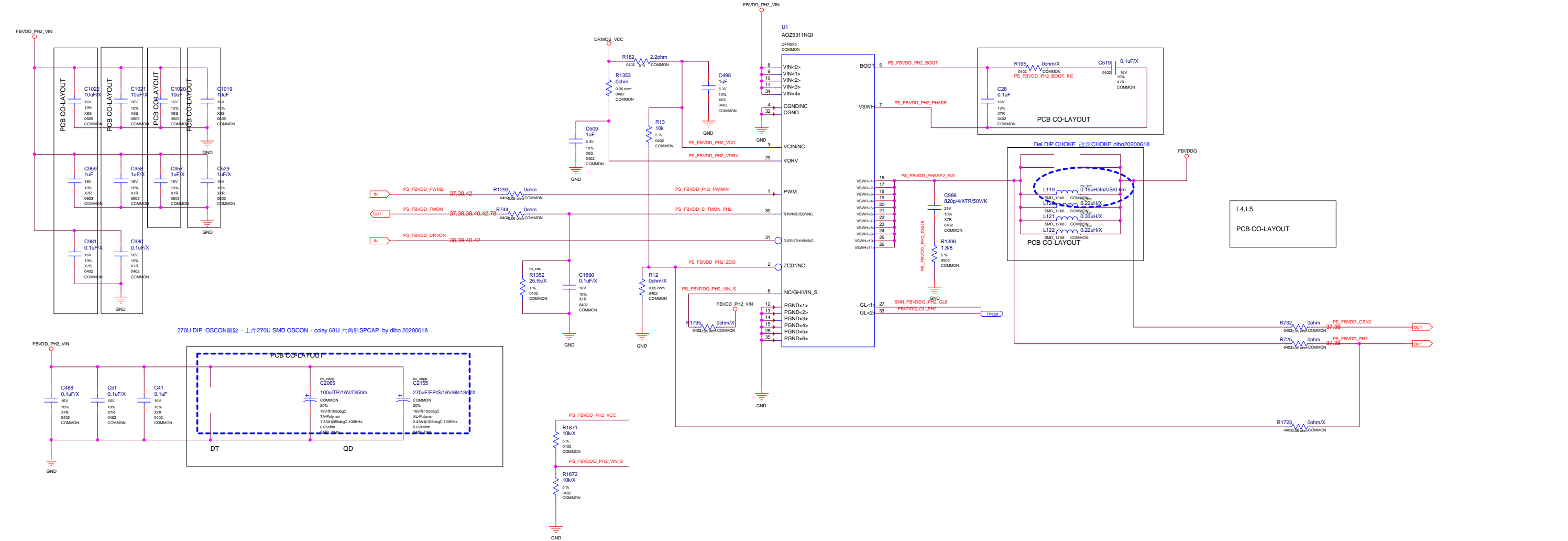
GIGABYTE			
Title PS: FBVDD PH1			
Size Custom	Document Number GV-N3080AORUS X-10GD		Rev 1.0
Date: Monday, September 28, 2020		Sheet 39	of 80

## PS: FBVDD PH3



### FBVDD PH3 INPUT ANTI-BACKDRIVE

PS: FBVDD PH2

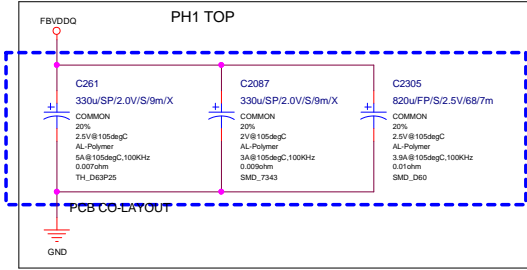




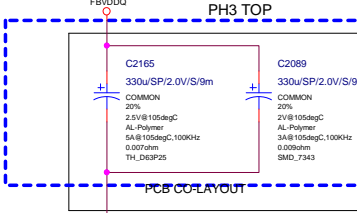
PS: FBVDD OUTPUT CAP

3x 820uF TH FBVDD OUTPUT BULK CAPS

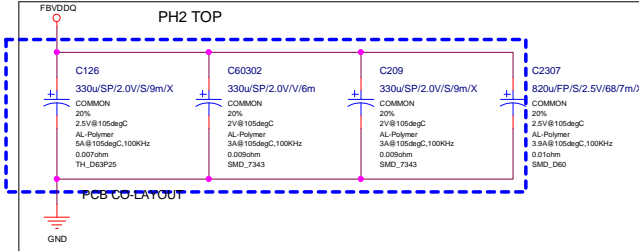
820U DIP OSCON 改330U 預留在BOT・原SMD OSCON改常用footprint上件820U by dho 20200619



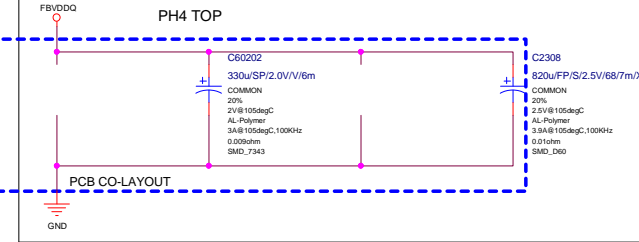
820U DIP OSCON 改330U SMD 7343 by dho 20200619



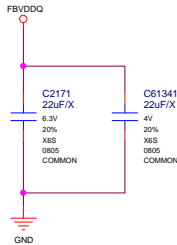
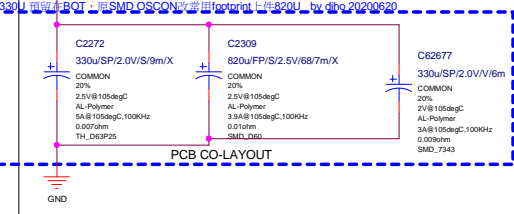
820U DIP OSCON 改330U 預留在BOT・原SMD OSCON改常用footprint上件820U by dho 20200619



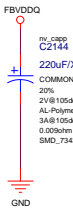
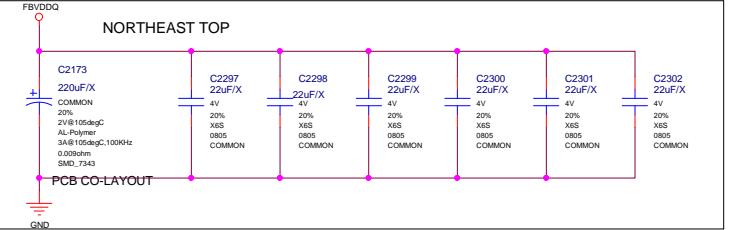
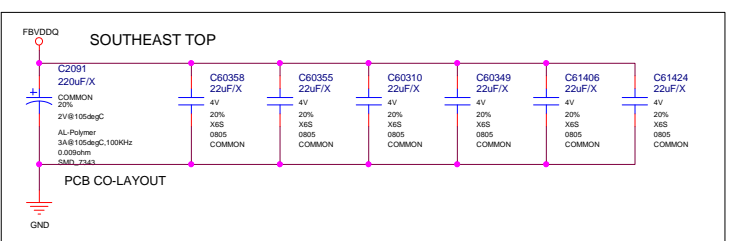
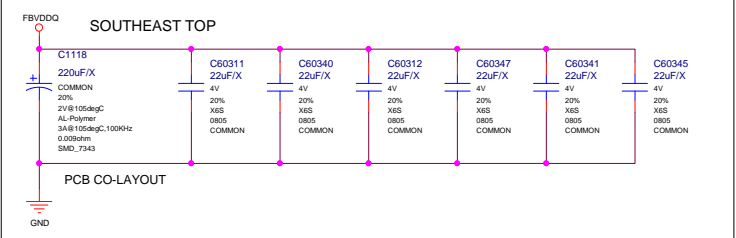
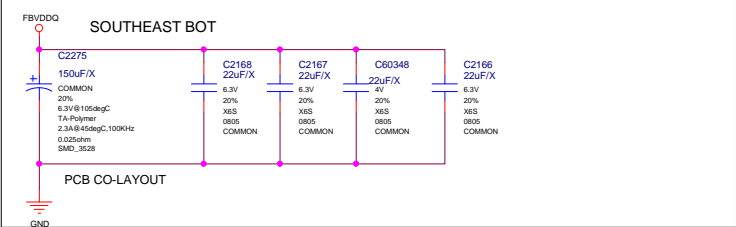
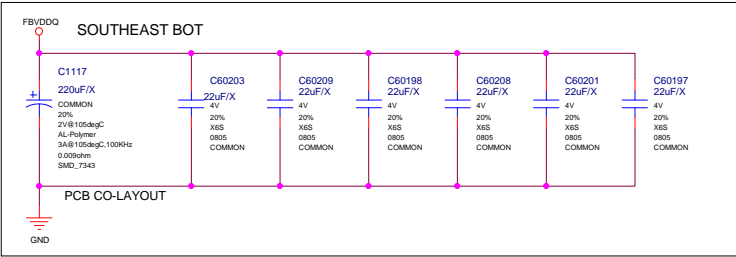
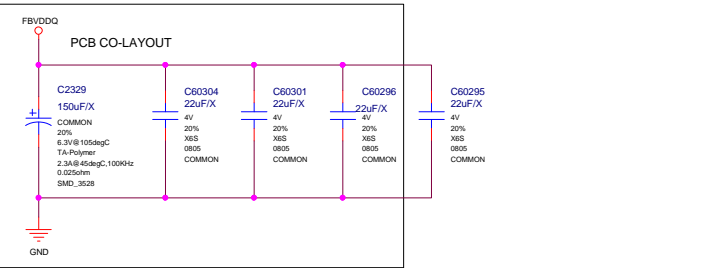
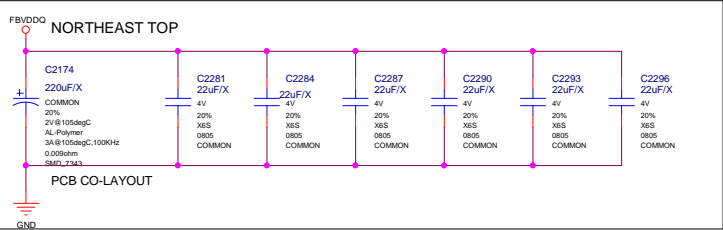
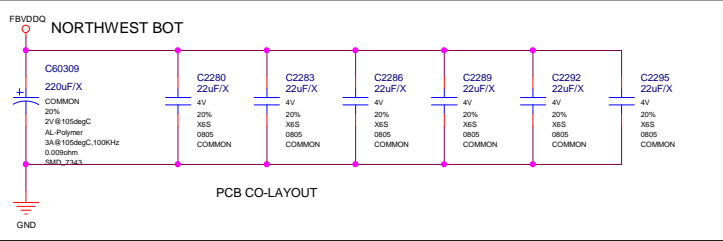
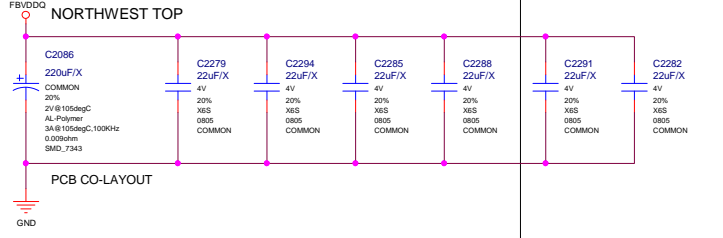
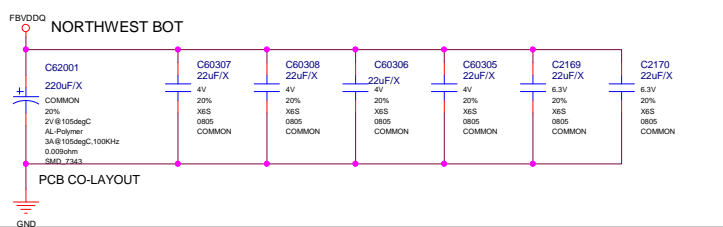
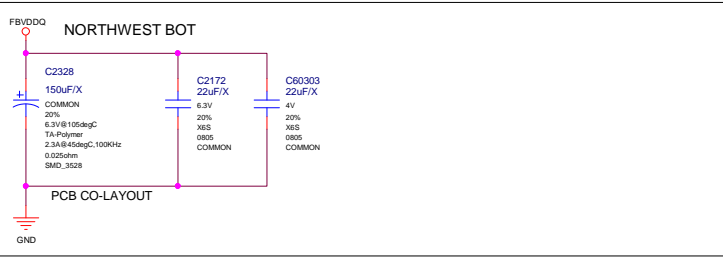
820U DIP OSCON 改330U 預留在BOT・原SMD OSCON改常用footprint上件820U by dho 20200619



新增 820U 預留在BOT・原SMD OSCON改常用footprint上件820U by dho 20200620



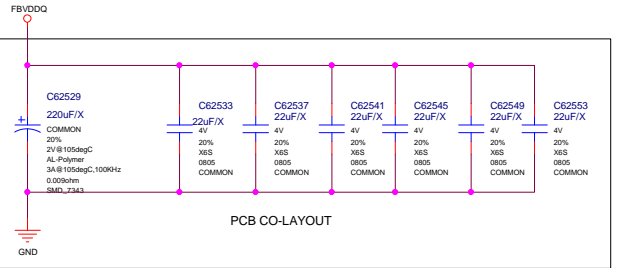
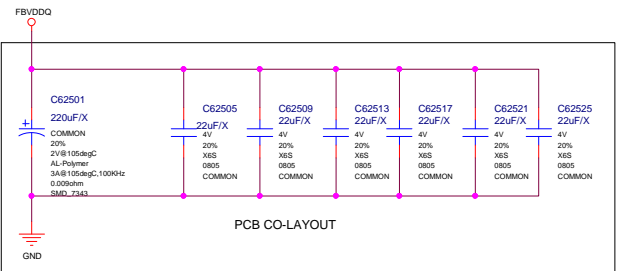
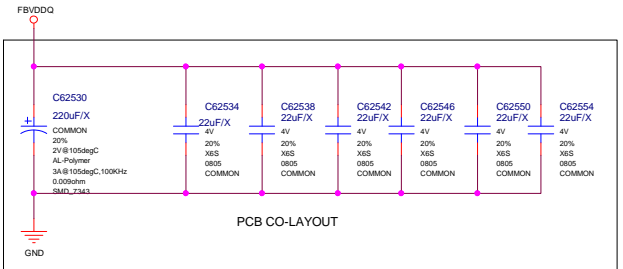
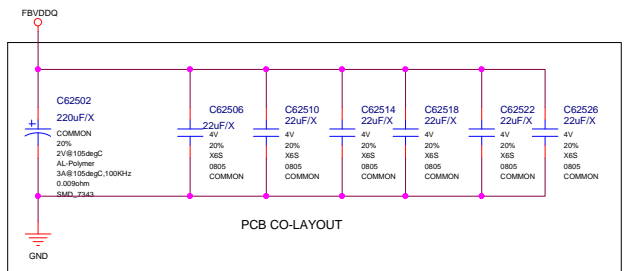
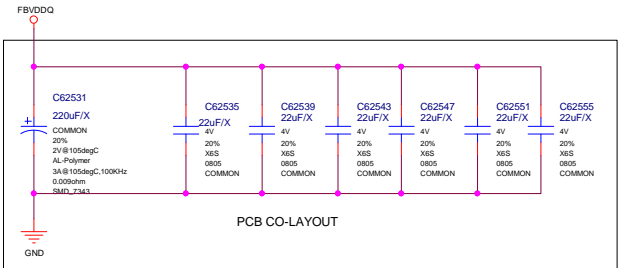
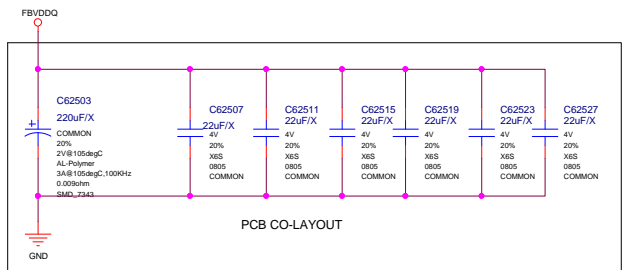
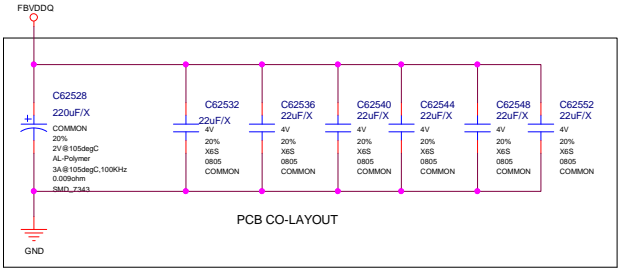
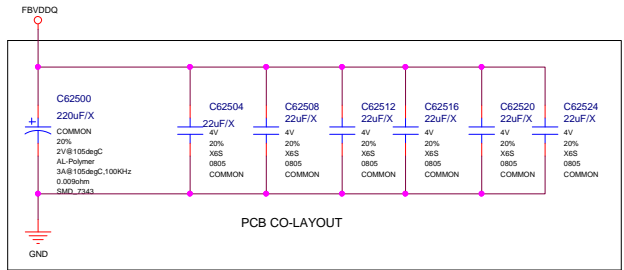
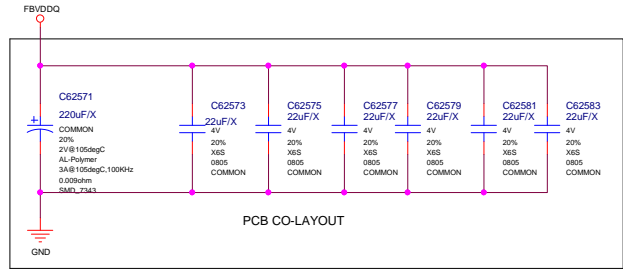
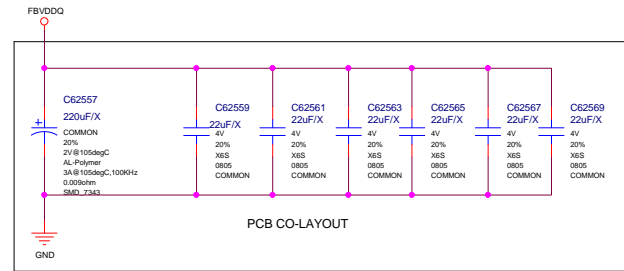
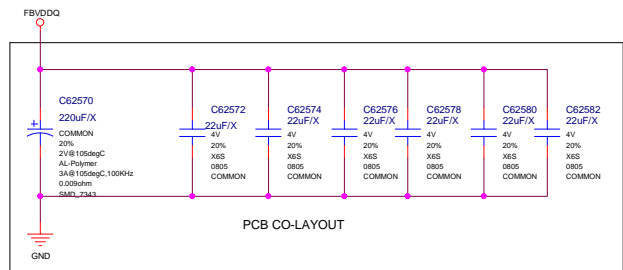
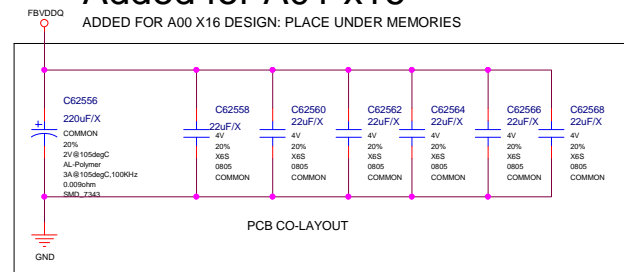
CLOSE TO FB PH3 OUTPUT STUFF





Added for A01 x16

ADDED FOR A00 X16 DESIGN: PLACE UNDER MEMORIES



ASSEMBLY  
PAGE DETAIL

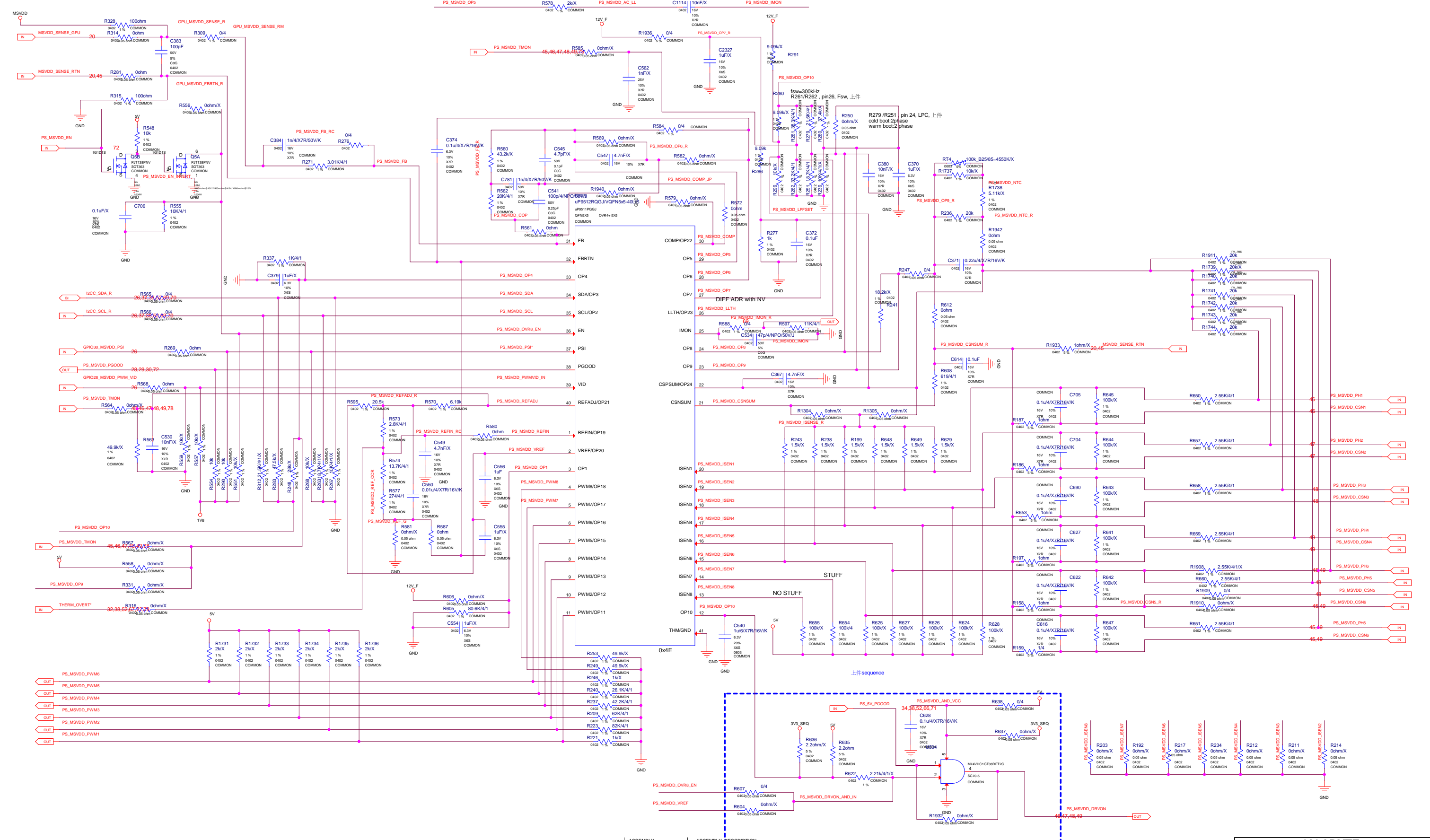
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GIGABYTE

Title			PS: FBVDD OUTPUT CAP_NEAR
Size	Document Number	Rev	
Custom	GV-N3080AORUS X-10GD	1.0	
Date:	Monday, September 28, 2020	Sheet	44 of 80

PS: MSVDD



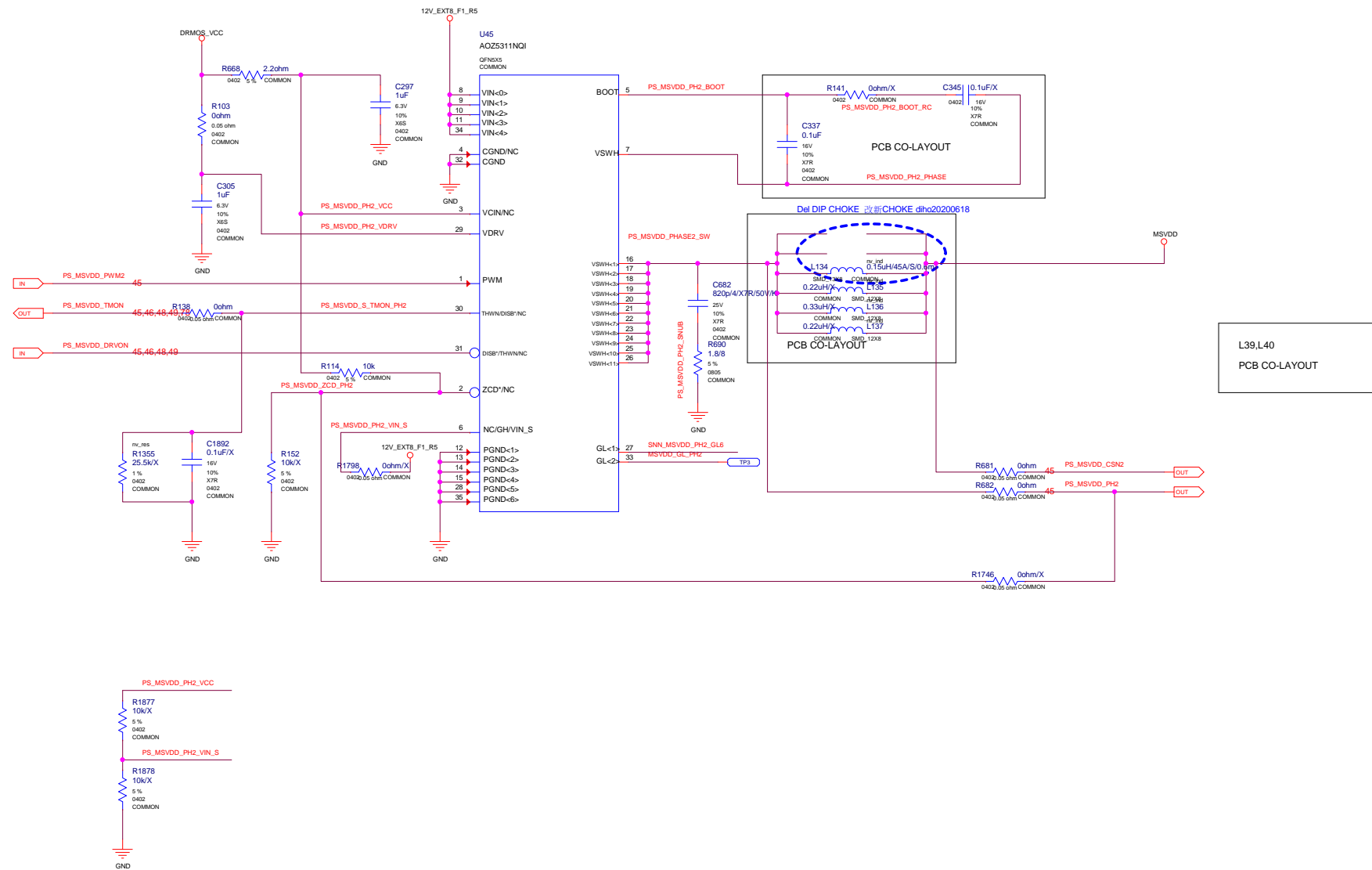
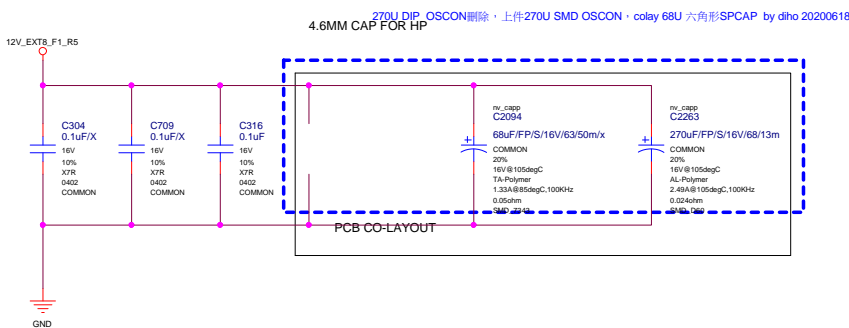
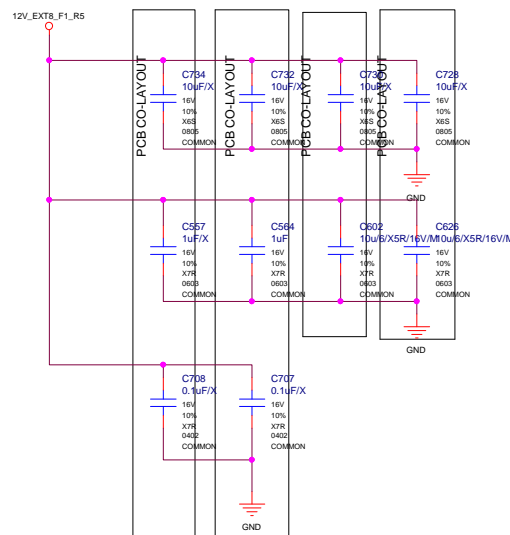
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GIGABYTE

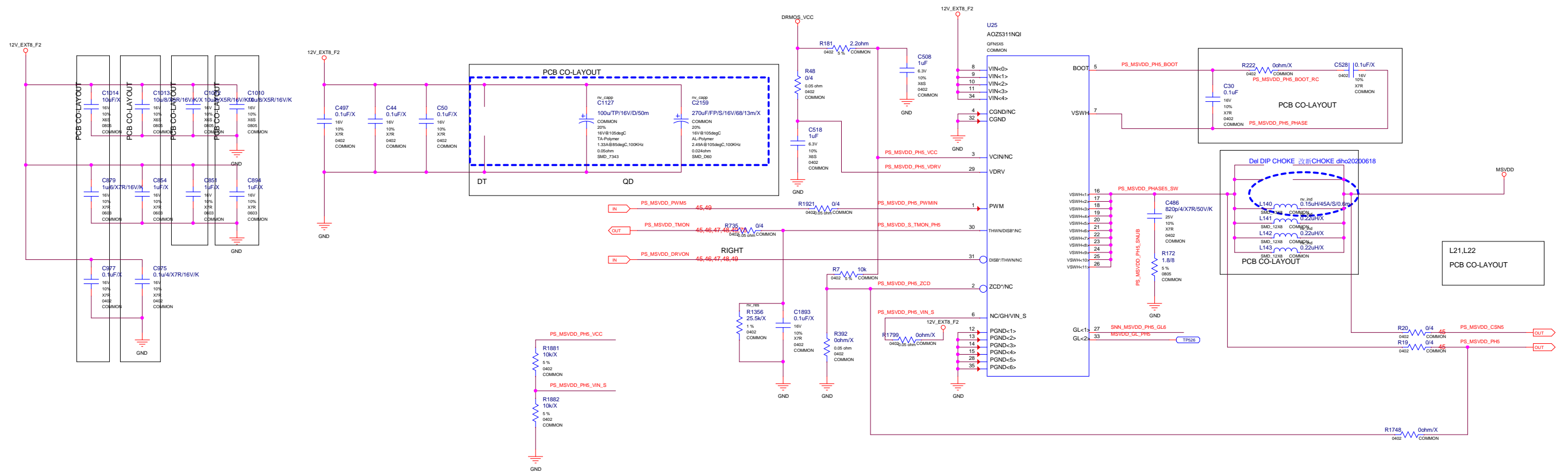
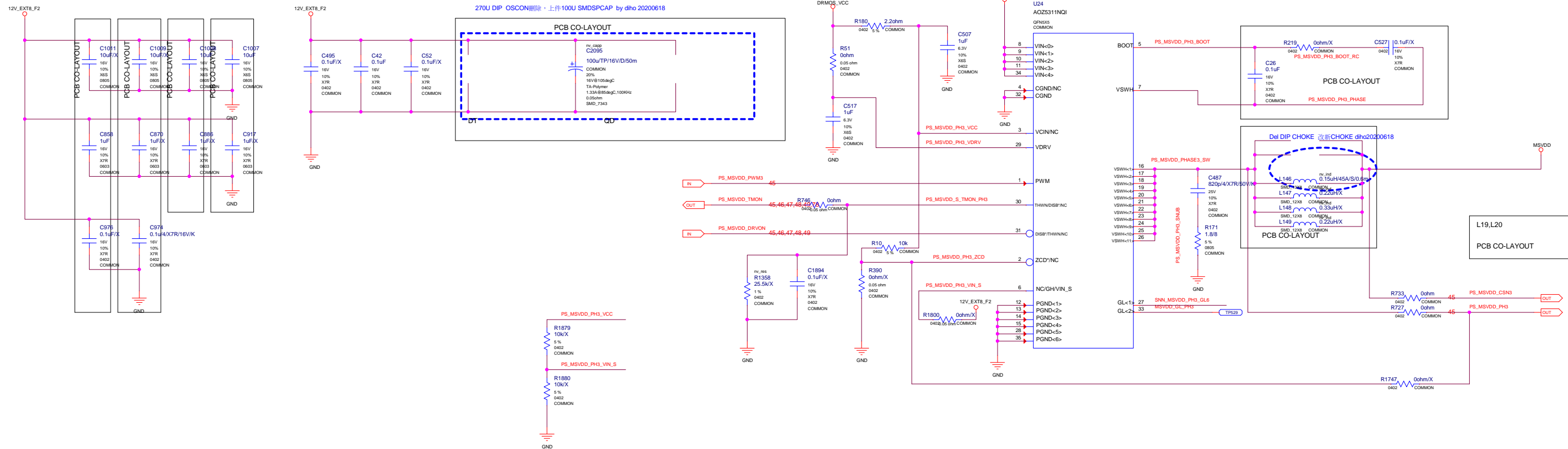
Title		PS: MSVDD	Rev	1.0
Size	Custom	Document Number		
GV-N3080AORUS X-10GD				
Date	Monday, September 26, 2020	Sheet		



## PS: MSVDD PH 2



## PS:MSVDD Phase 3, 5



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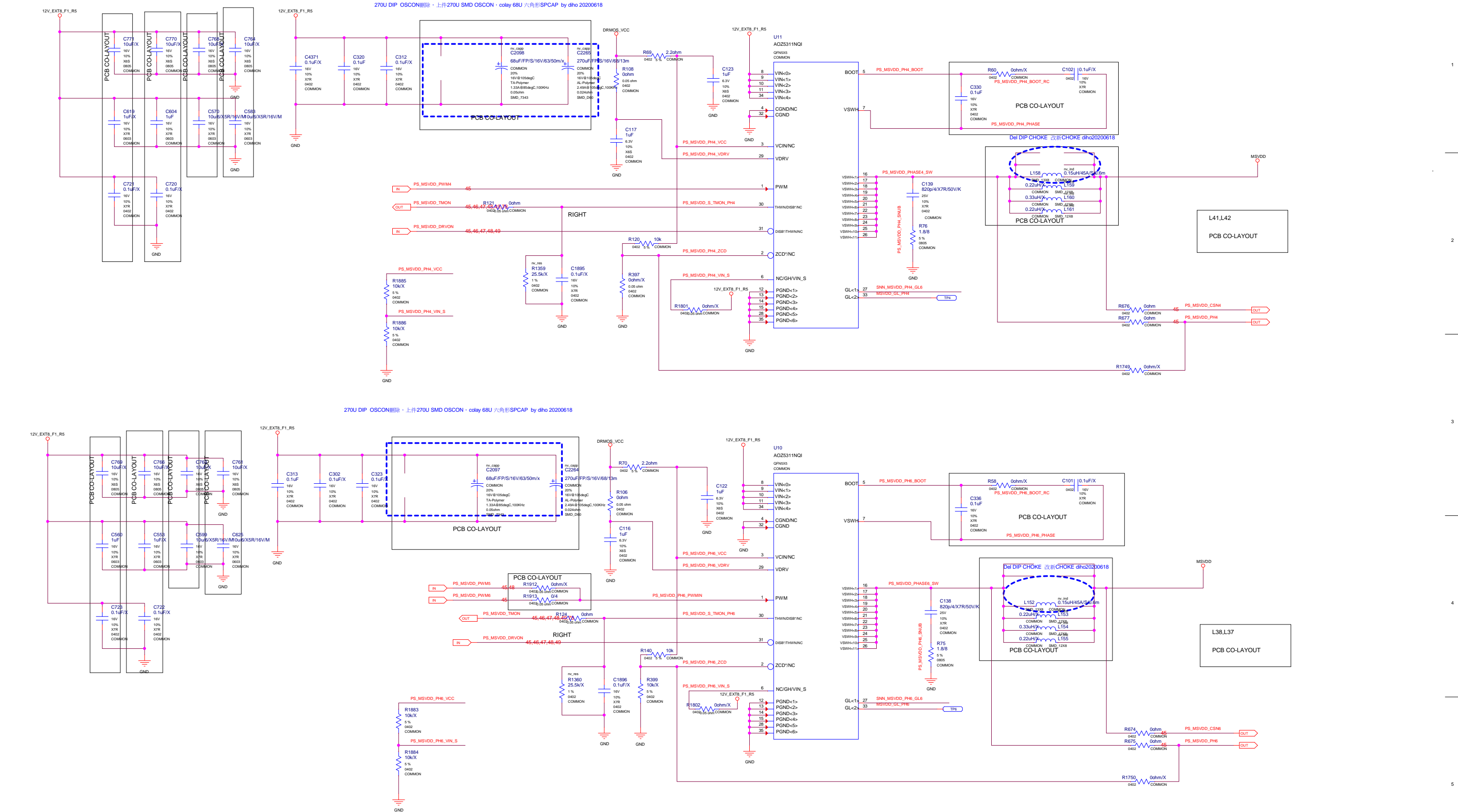
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## GIGABYTE

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PS: MSVDD Phase 3,5			
Size	Document Number		Rev
Custom	GV-N3080AORUS X-10GD		1.0
Date:	Monday, September 26, 2020	Sheet	48 of 80

PS: MSVDD PH 4,6



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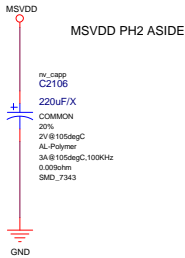
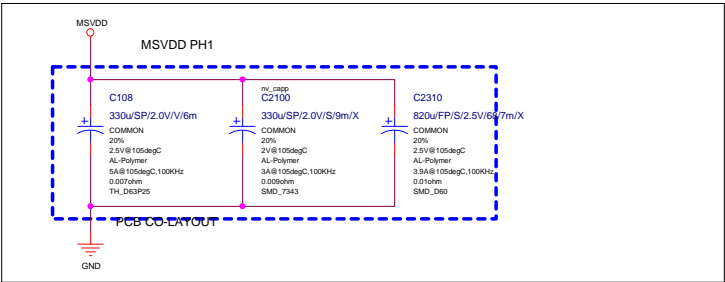
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PS: MSVDD PH4 and PH6

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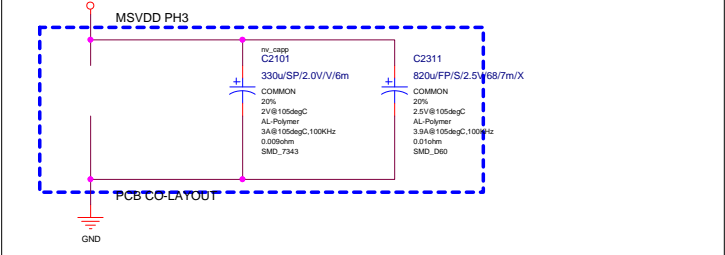
Title PS: MSVDD Phase 4,6		
Size Custom	Document Number GV-N3080AORUS X-10GD	Rev 1.0
Date: Monday, September 28, 2020	Sheet 49	of 80

PS:MSVDD OUTPUT CAP (TOP)

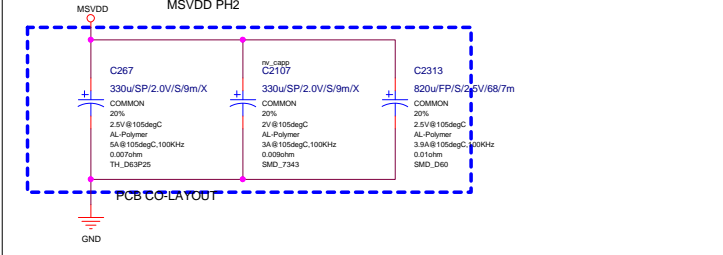
820U DIP OSCON 改330U 预留在BOT，原SMD OSCON改常用footprint上件820U by diho 20200619



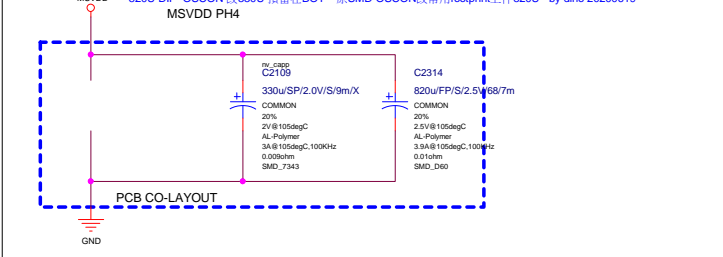
820U DIP OSCON 改330U 预留在BOT，原SMD OSCON改常用footprint上件820U by diho 20200619



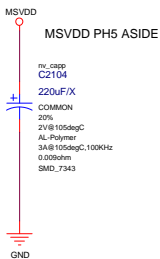
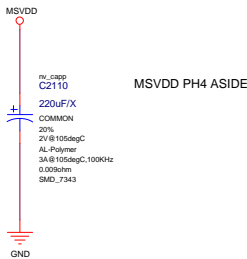
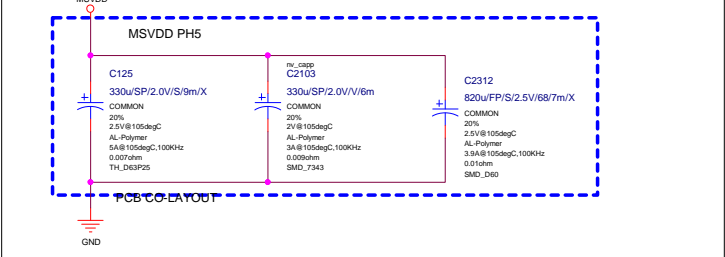
820U DIP OSCON 改330U 预留在BOT，原SMD OSCON改常用footprint上件820U by diho 20200619



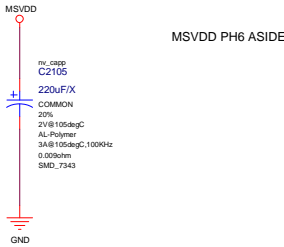
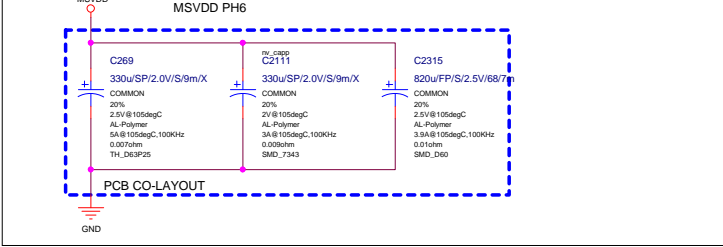
820U DIP OSCON 改330U 预留在BOT，原SMD OSCON改常用footprint上件820U by diho 20200619



820U DIP OSCON 改330U 预留在BOT，原SMD OSCON改常用footprint上件820U by diho 20200619



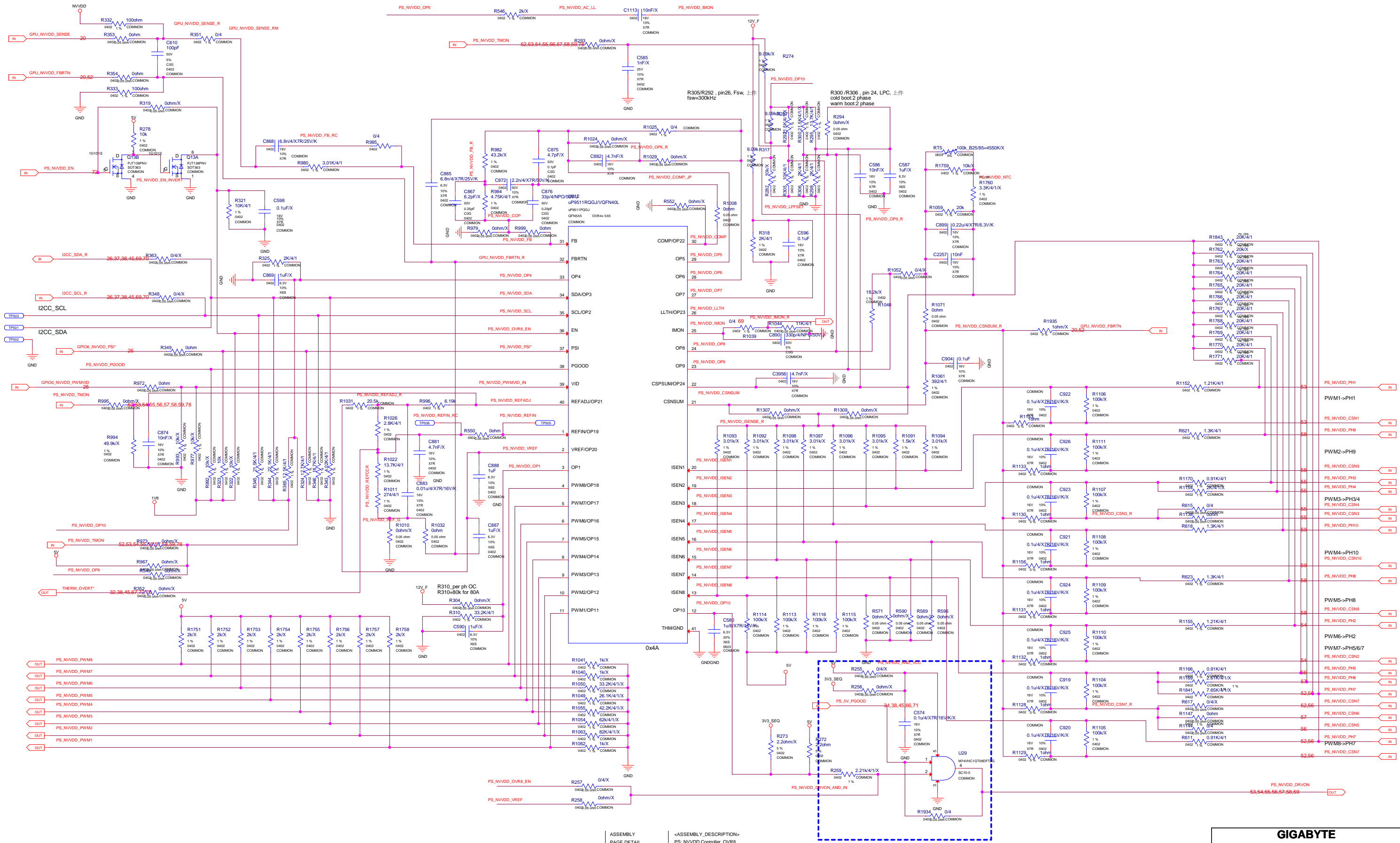
820U DIP OSCON 改330U 预留在BOT，原SMD OSCON改常用footprint上件820U by diho 20200619





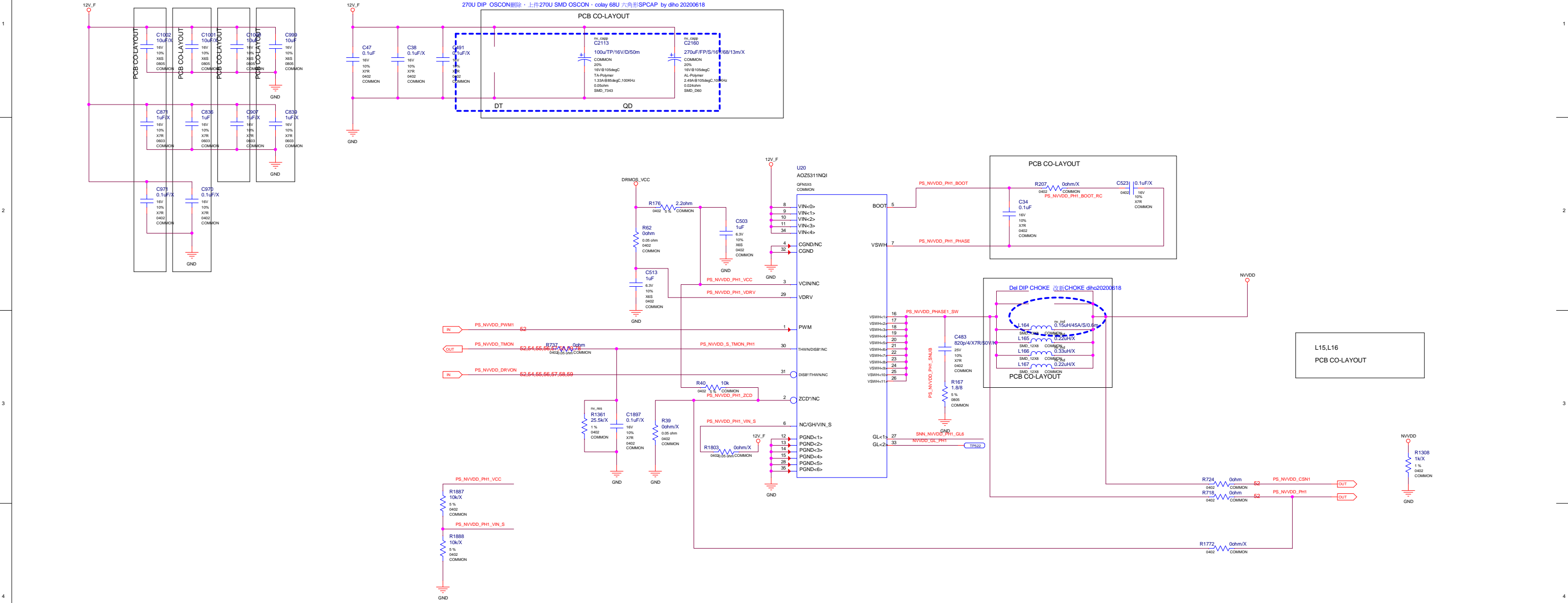


## PS: NVVDD Controller\_OVR8



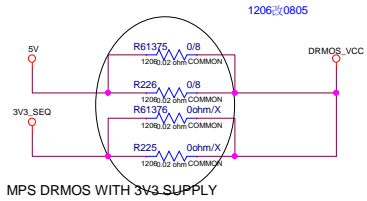
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PS: NVVDD Phase 1

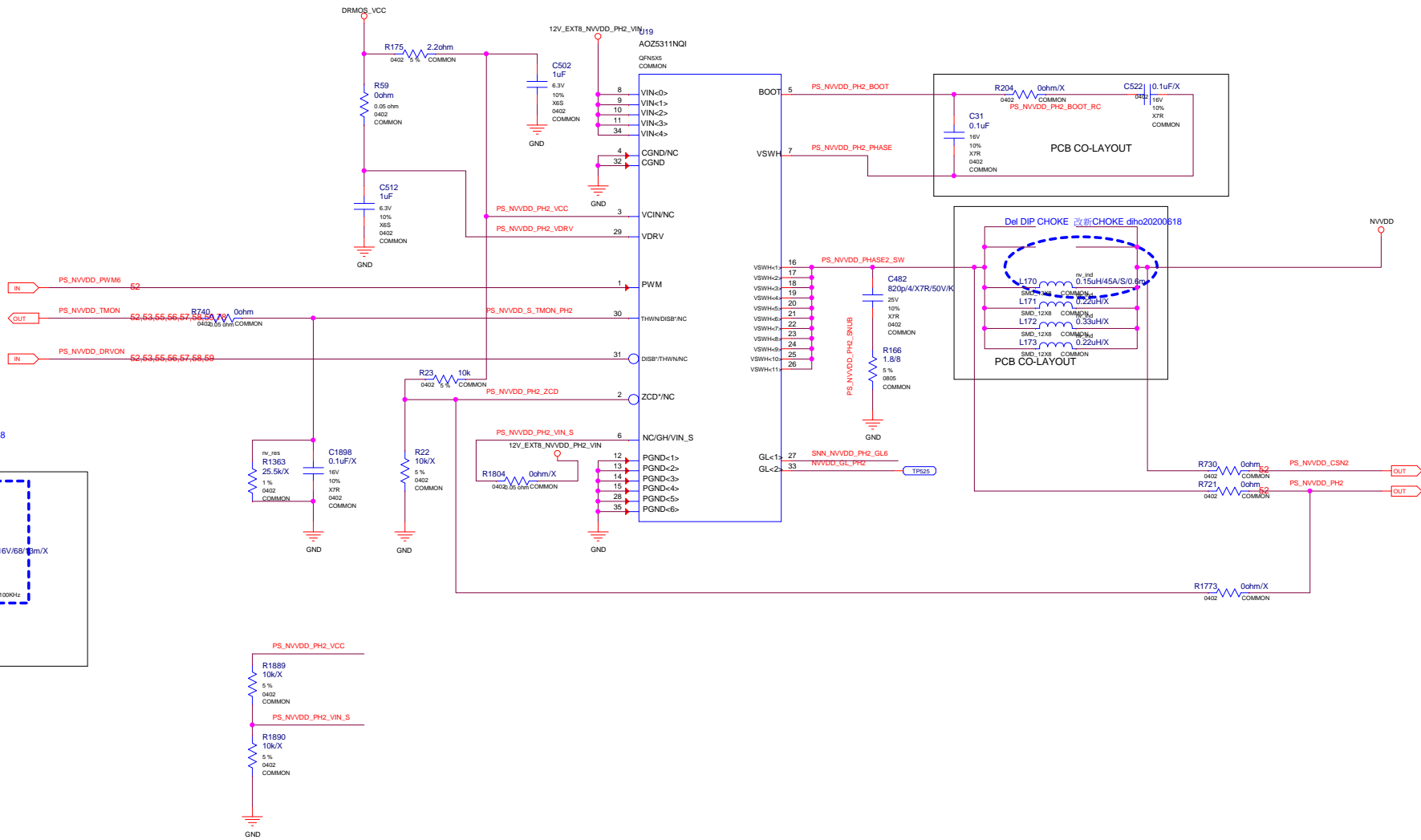
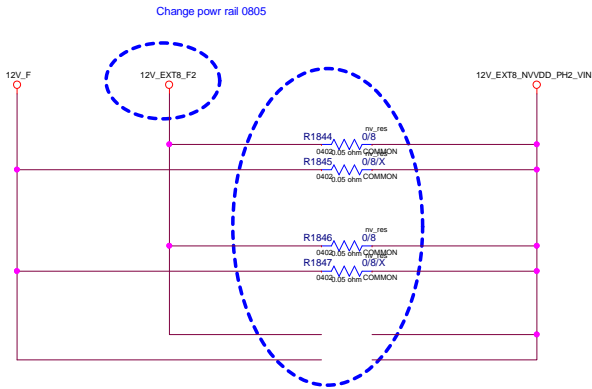
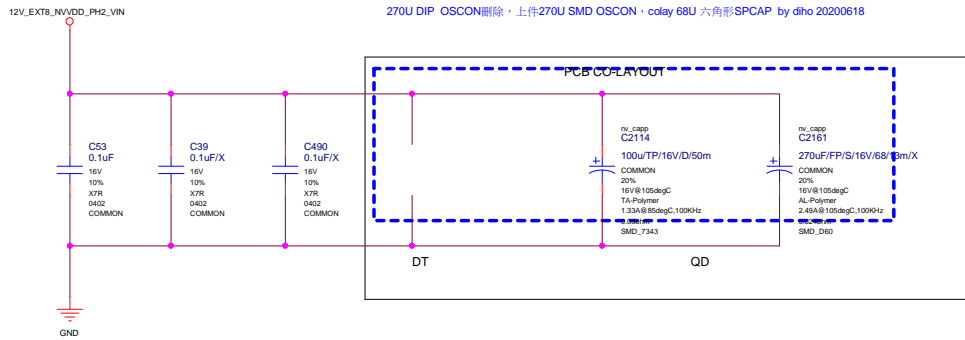
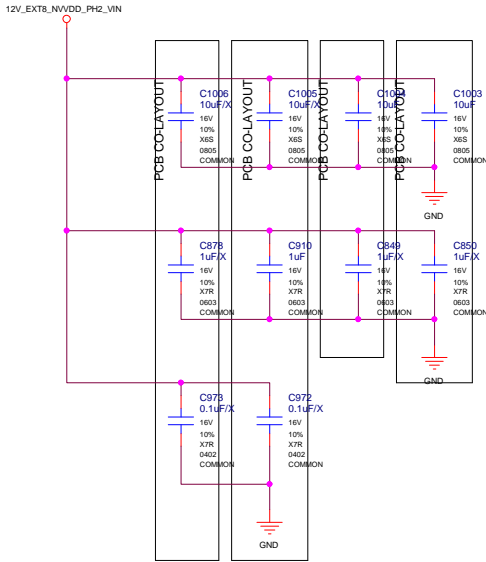


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PS: NVVDD Phase 2



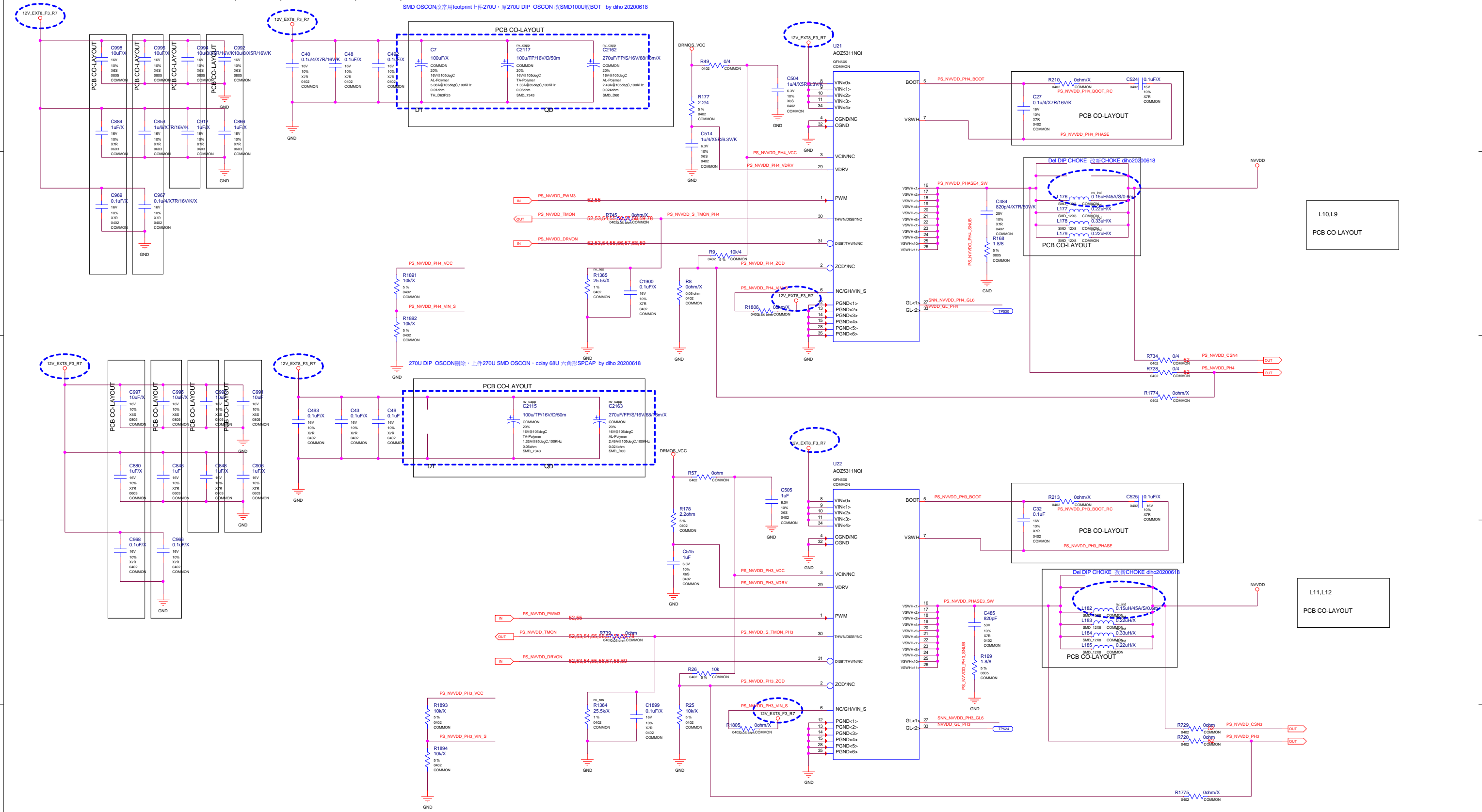
MPS DRMos WITH 3V3 SUPPLY



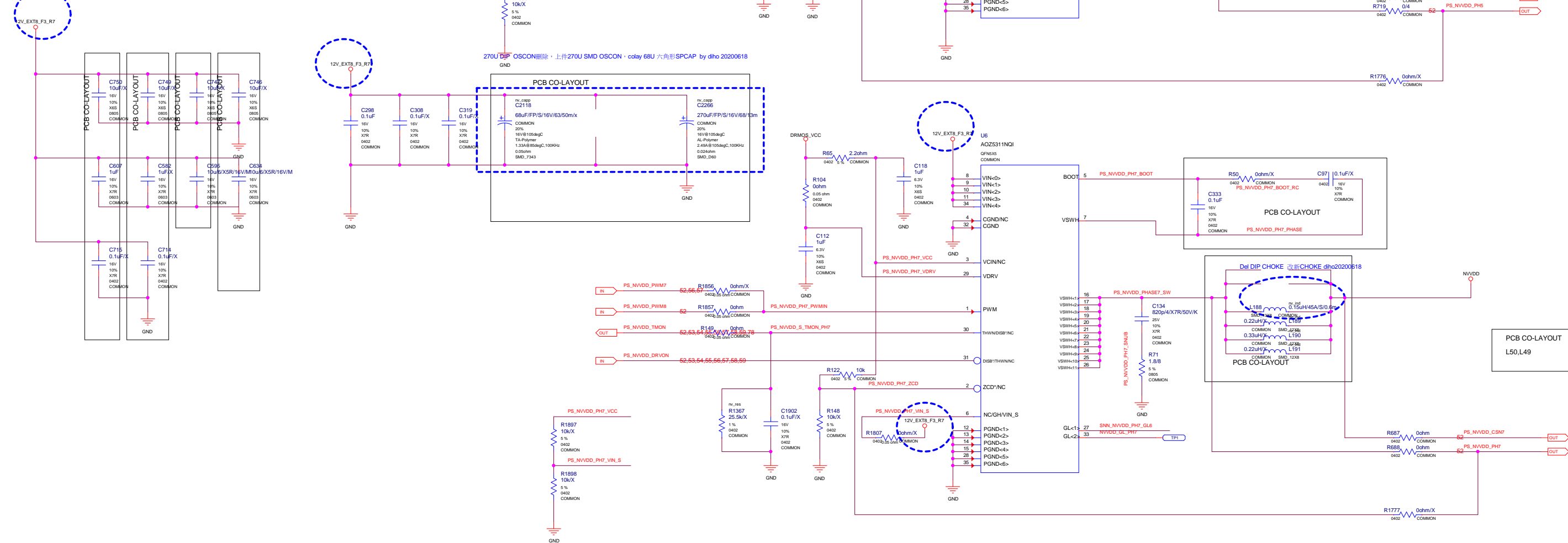
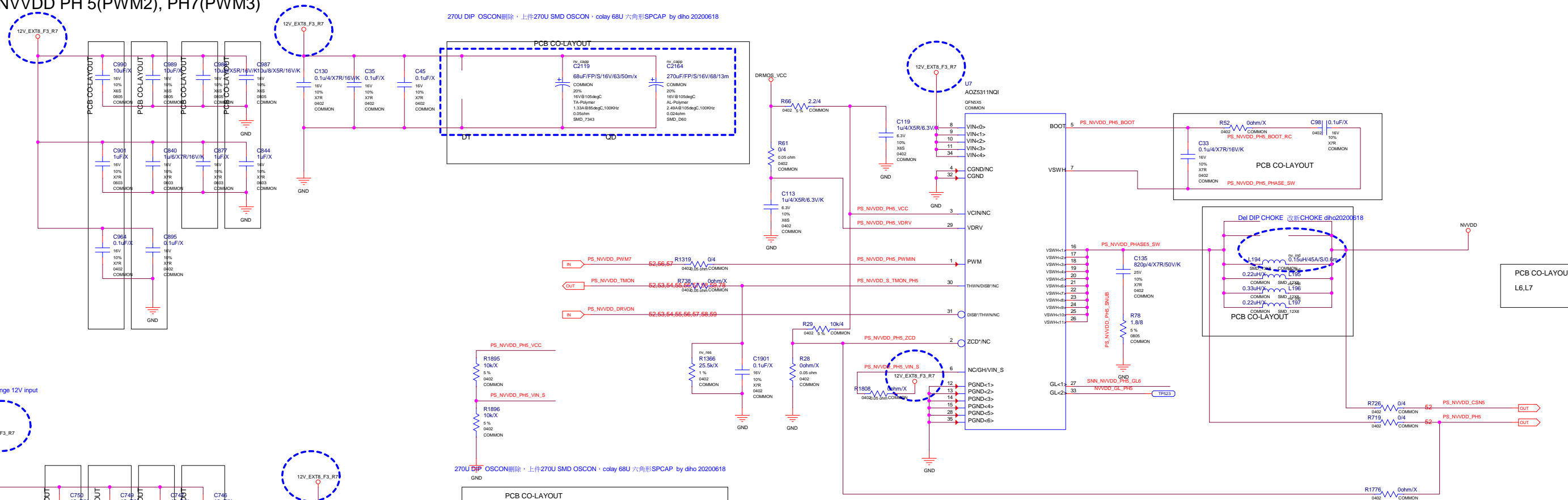
L13,L14  
PCB CO-LAYOUT

PS: NVVDD Phase 3 (PWM6), PHASE 4(PWM2)

SMD OSCON改常用footprint上件270U · 原270U DIP OSCON 改SMD100U改BOT by dho 20200618



PS: NVVDD PH 5(PWM2), PH7(PWM3)



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PS: NVVDD PH5(PWM7) and  
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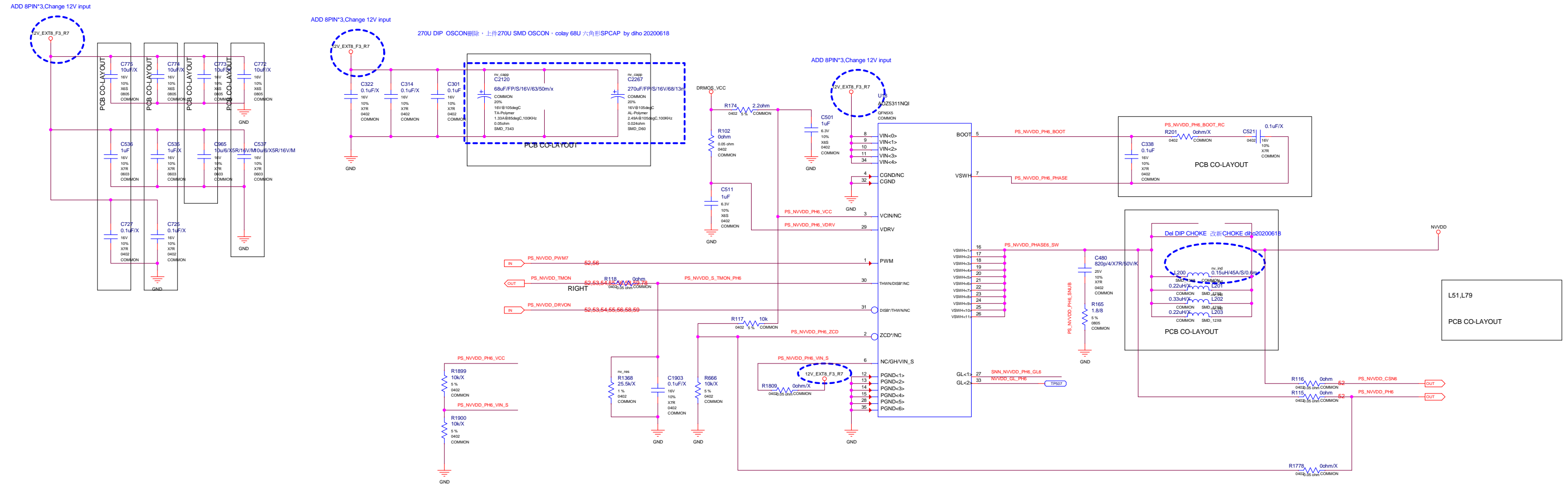
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Rev  
1.0

## PS: NVVDD Phase 6(PWM7)



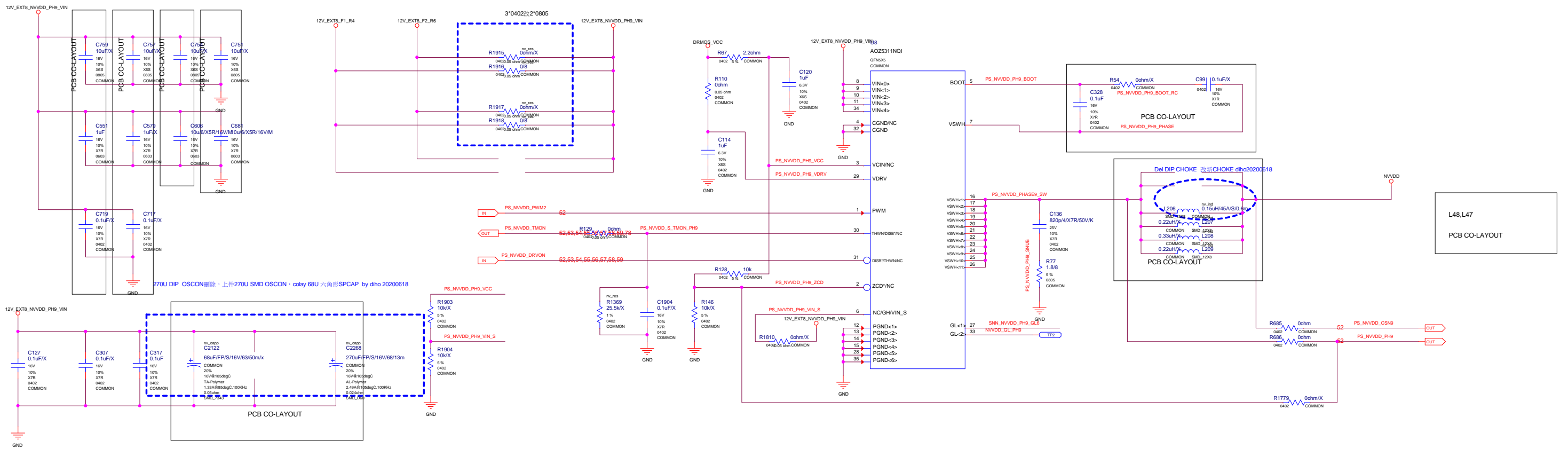
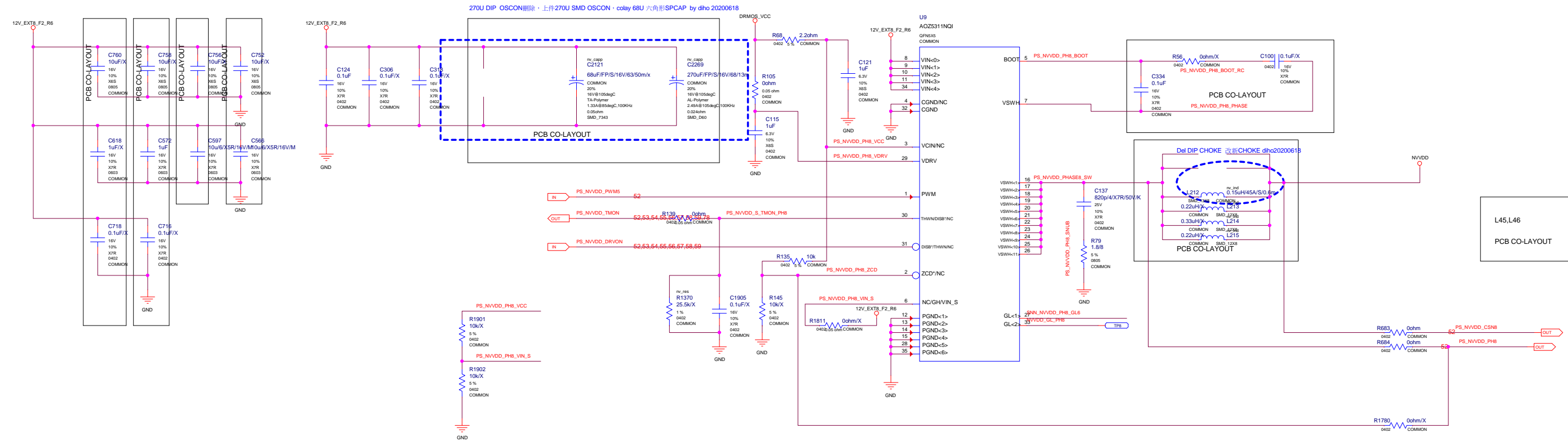
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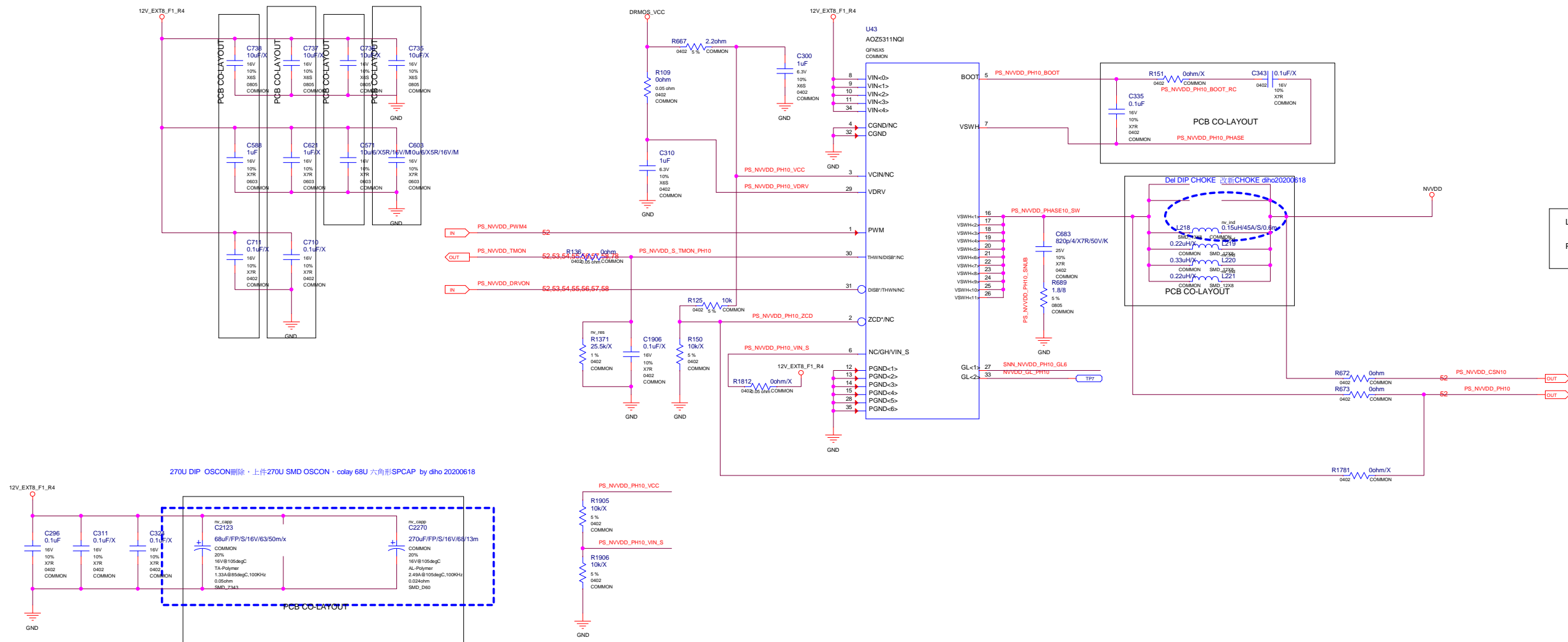


PS: NVVDD PH 8 (PWM5), PH 9(PWM8)



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## PS: NVVDD Phase 10 (PWM8)



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2								2
3								3
4								4
5								5

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PCB CO-LAYOUT

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PCB CO-LAYOUT

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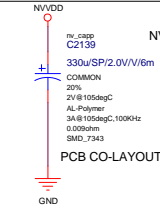
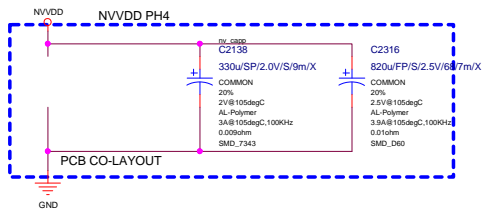
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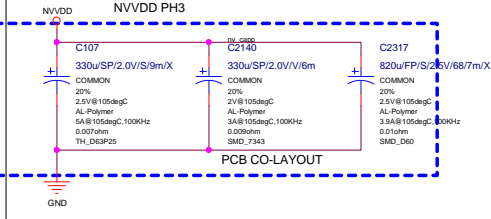
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Date:	Monday, September 28, 2020	Sheet	61 of 80

PS: NVVDD OUTPUT CAP(TOP)

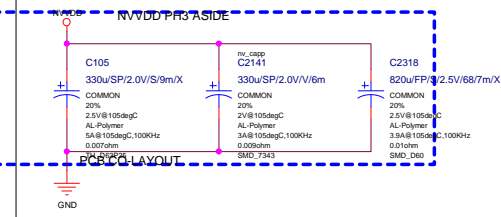
820U DIP OSCON 改330U 預留在BOT，原SMD OSCON改常用footprint上件820U by diho 20200619



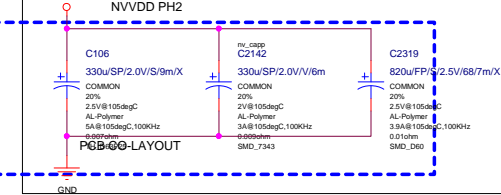
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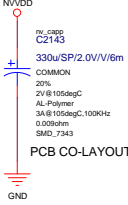
820U DIP OSCON 改330U 預留在BOT，原SMD OSCON改常用footprint上件820U by diho 20200619



820U DIP OSCON 改330U 預留在BOT，原SMD OSCON改常用footprint上件820U by diho 20200619



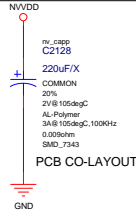
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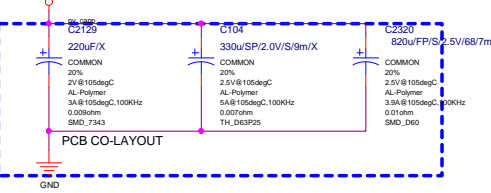
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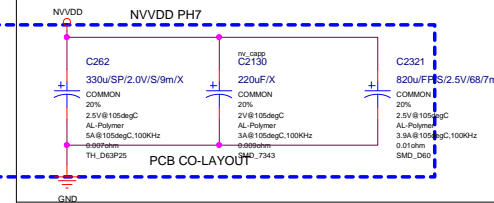
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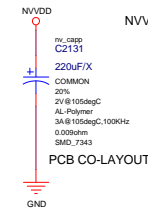
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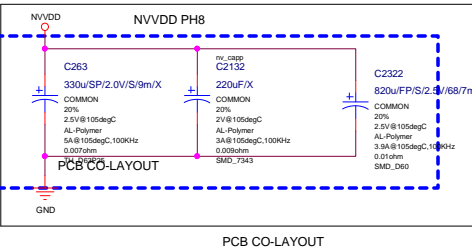
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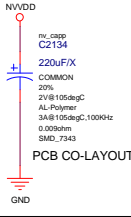
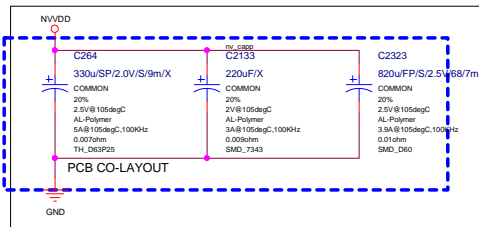
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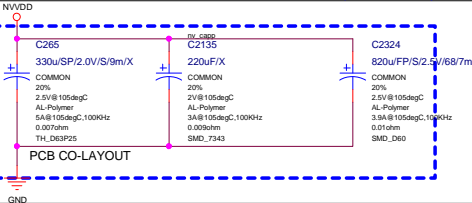
820U DIP OSCON 改330U 預留在BOT，原SMD OSCON改常用footprint上件820U by diho 20200619



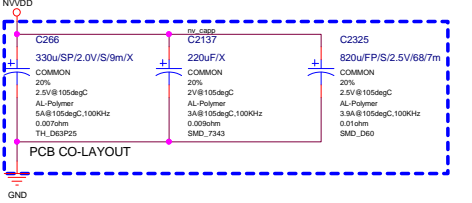
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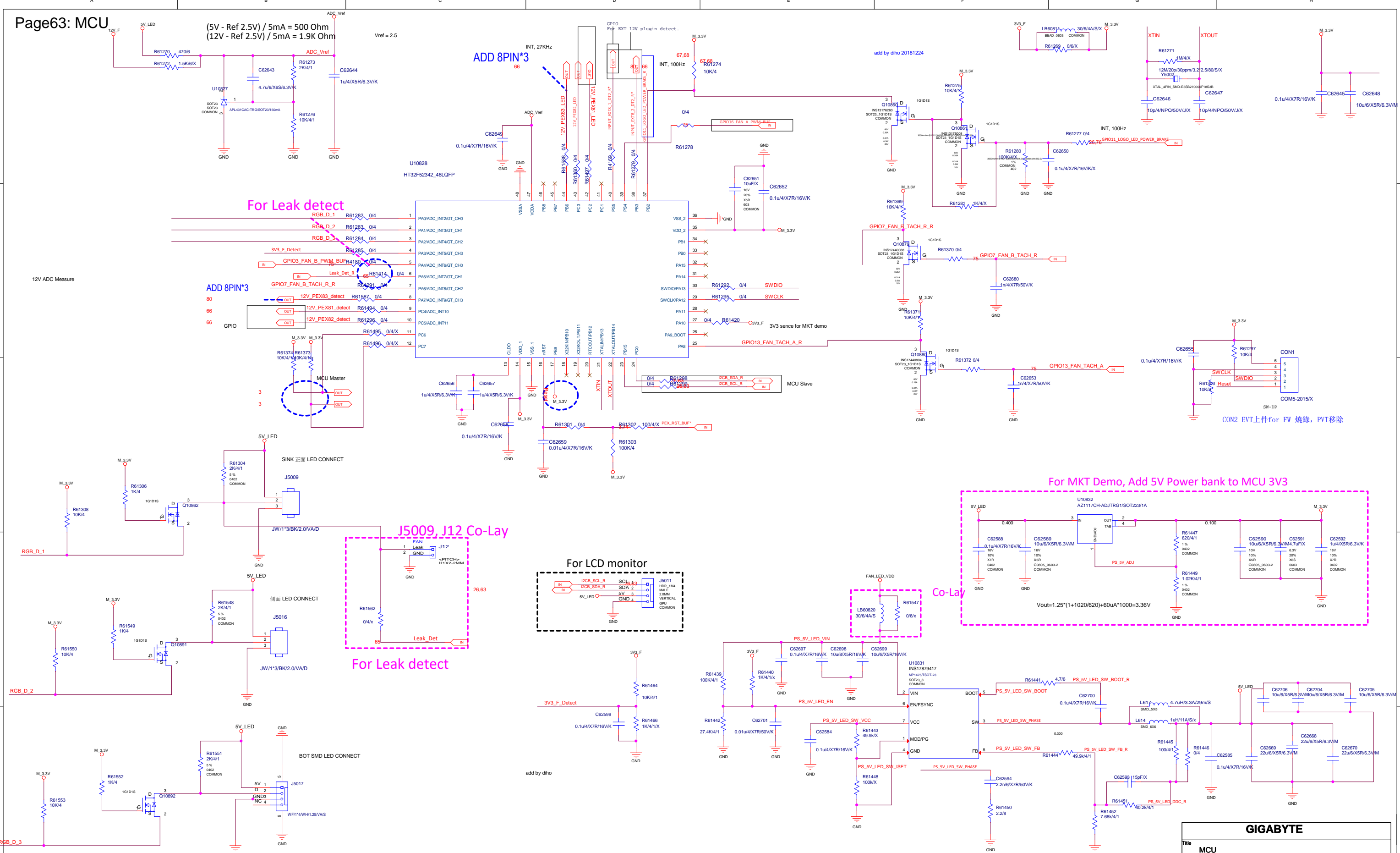
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820U DIP OSCON 改330U 預留在BOT，原SMD OSCON改常用footprint上件820U by diho 20200619



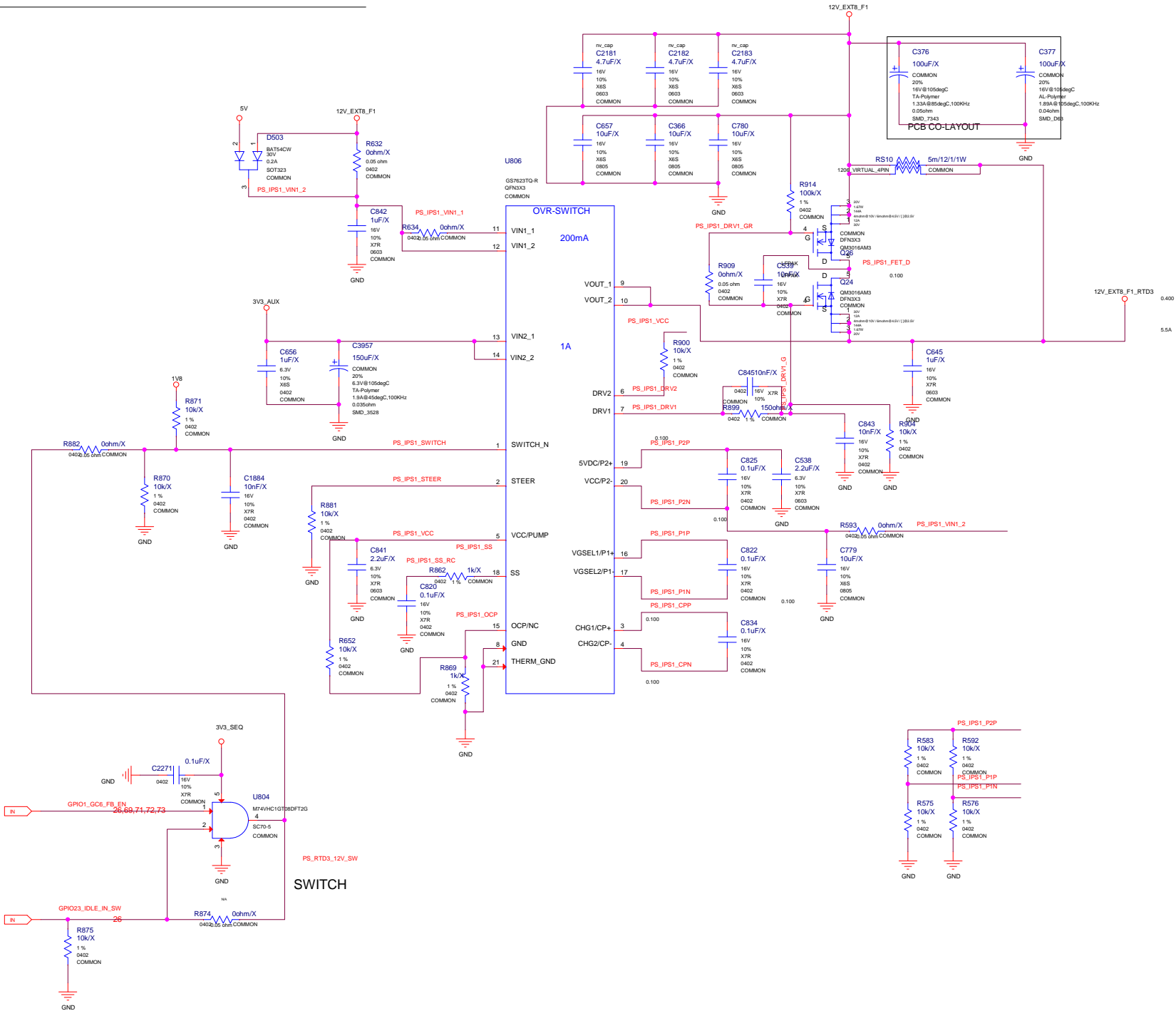
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PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

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1	0	0	12V_F
1	1	1	3V3A



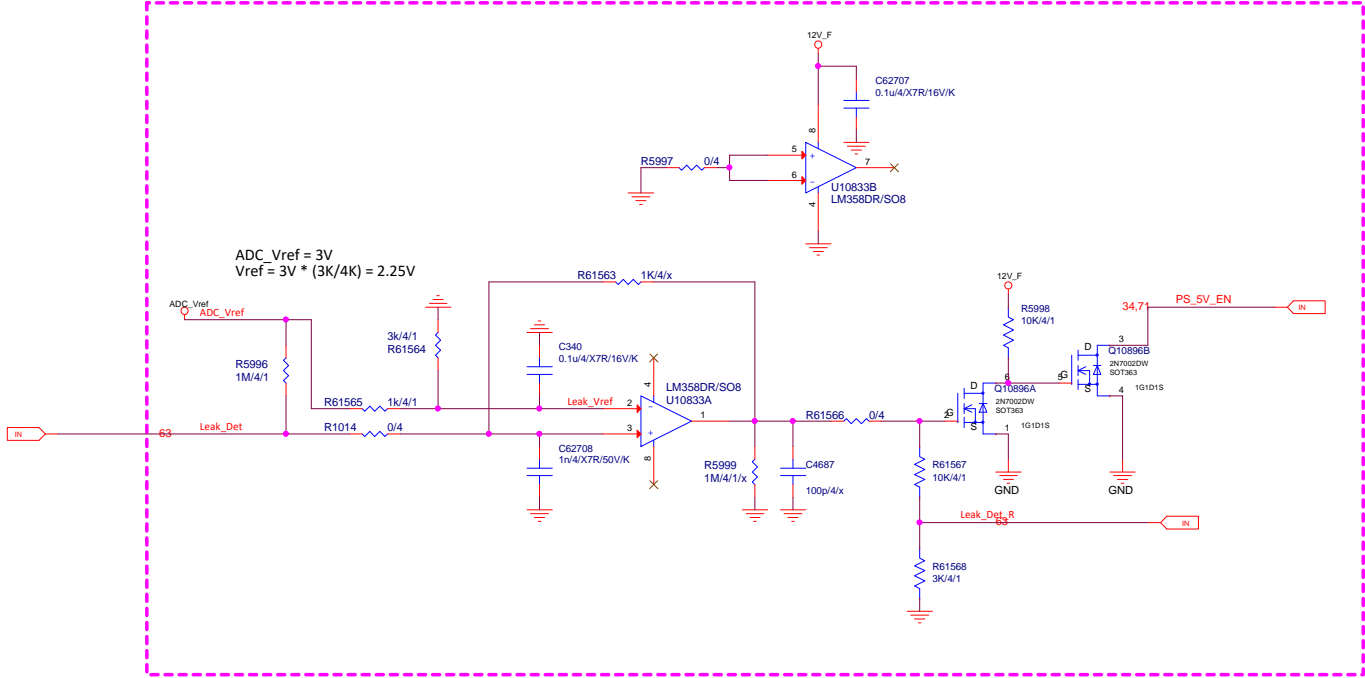
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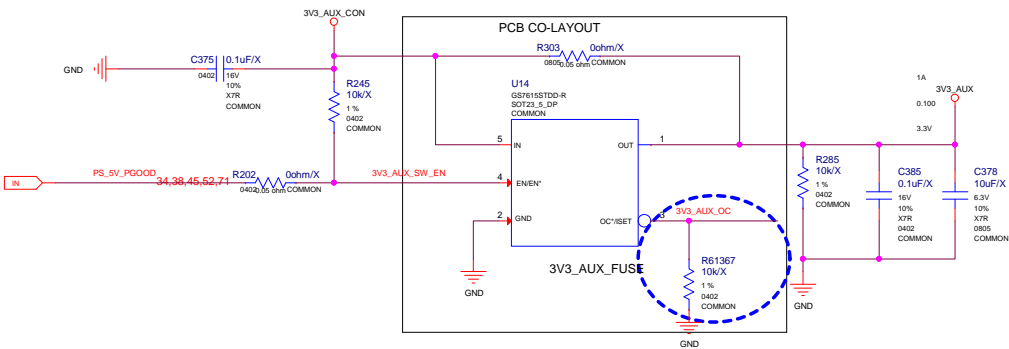
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Size Custom	Document Number GV-N3080AORUS X-10GD		Rev 1.0
Date: Monday, September 28, 2020	Sheet 64	of 80	



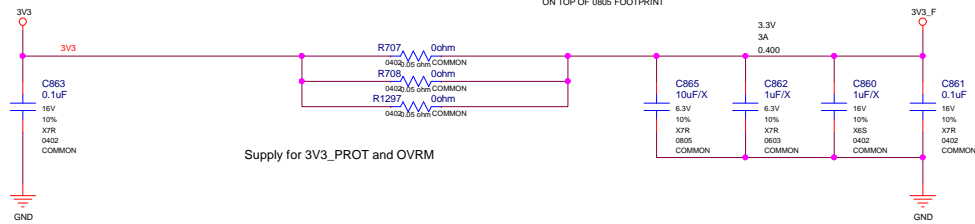
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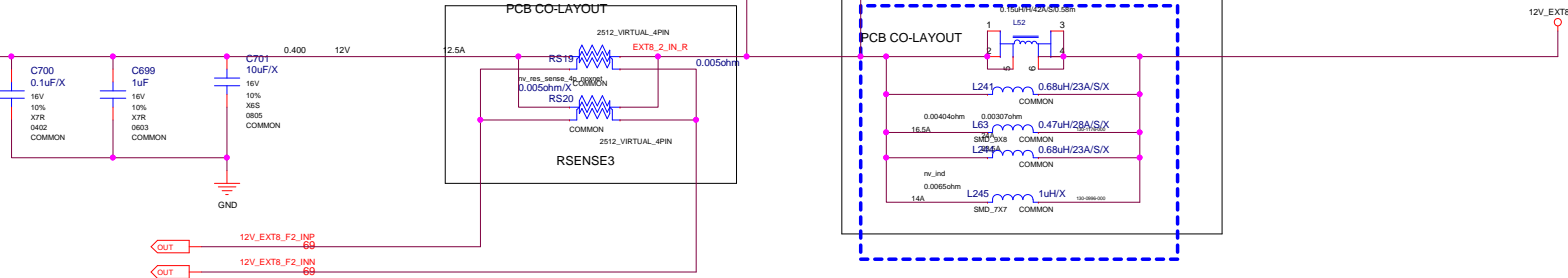
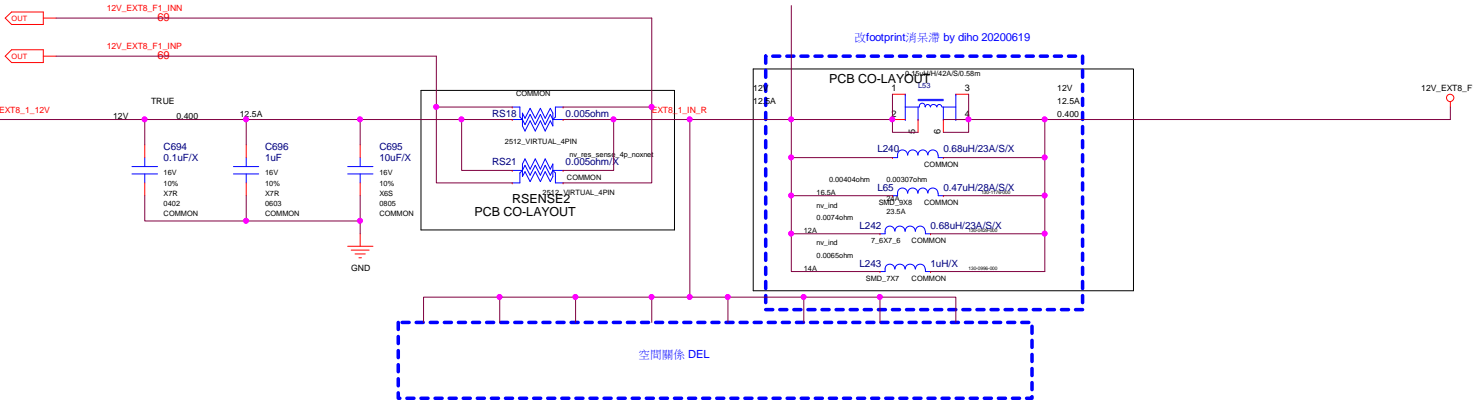
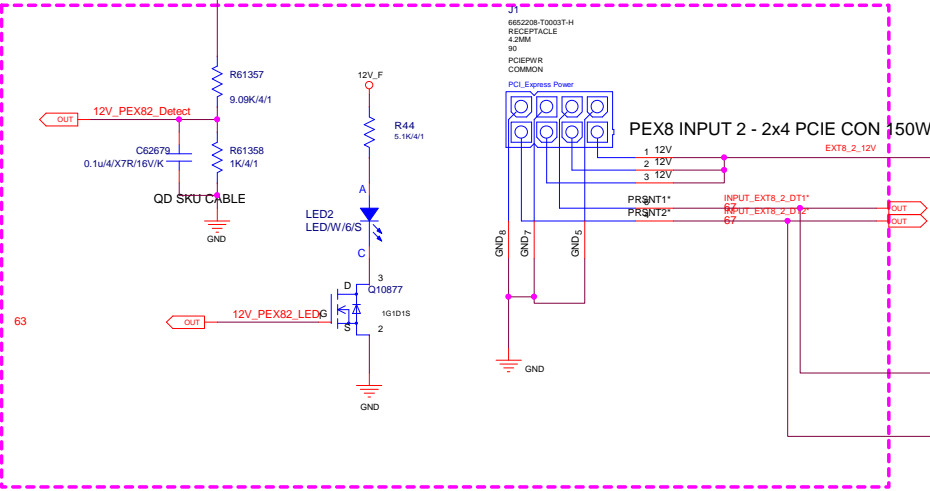
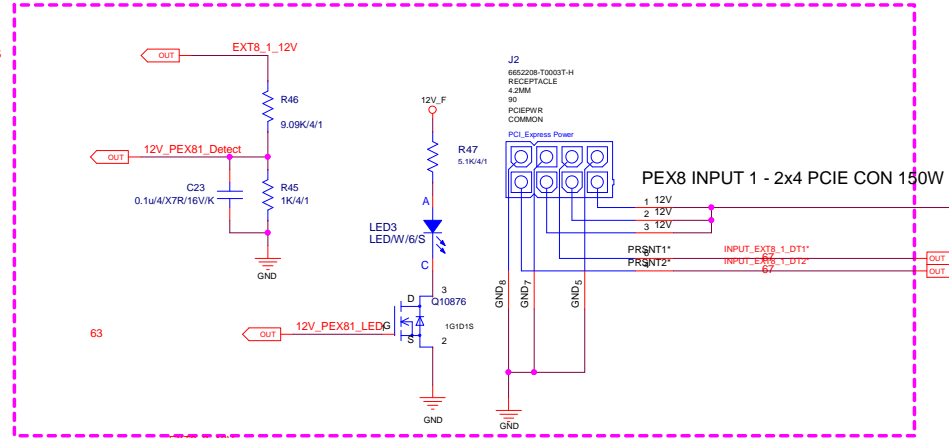
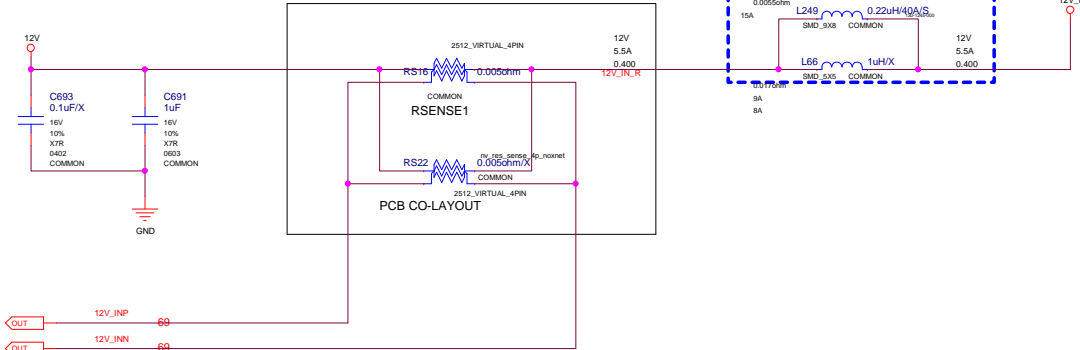
PS: Inputs, Filtering, and Monitoring



PEX 3V3 INPUT - 10W

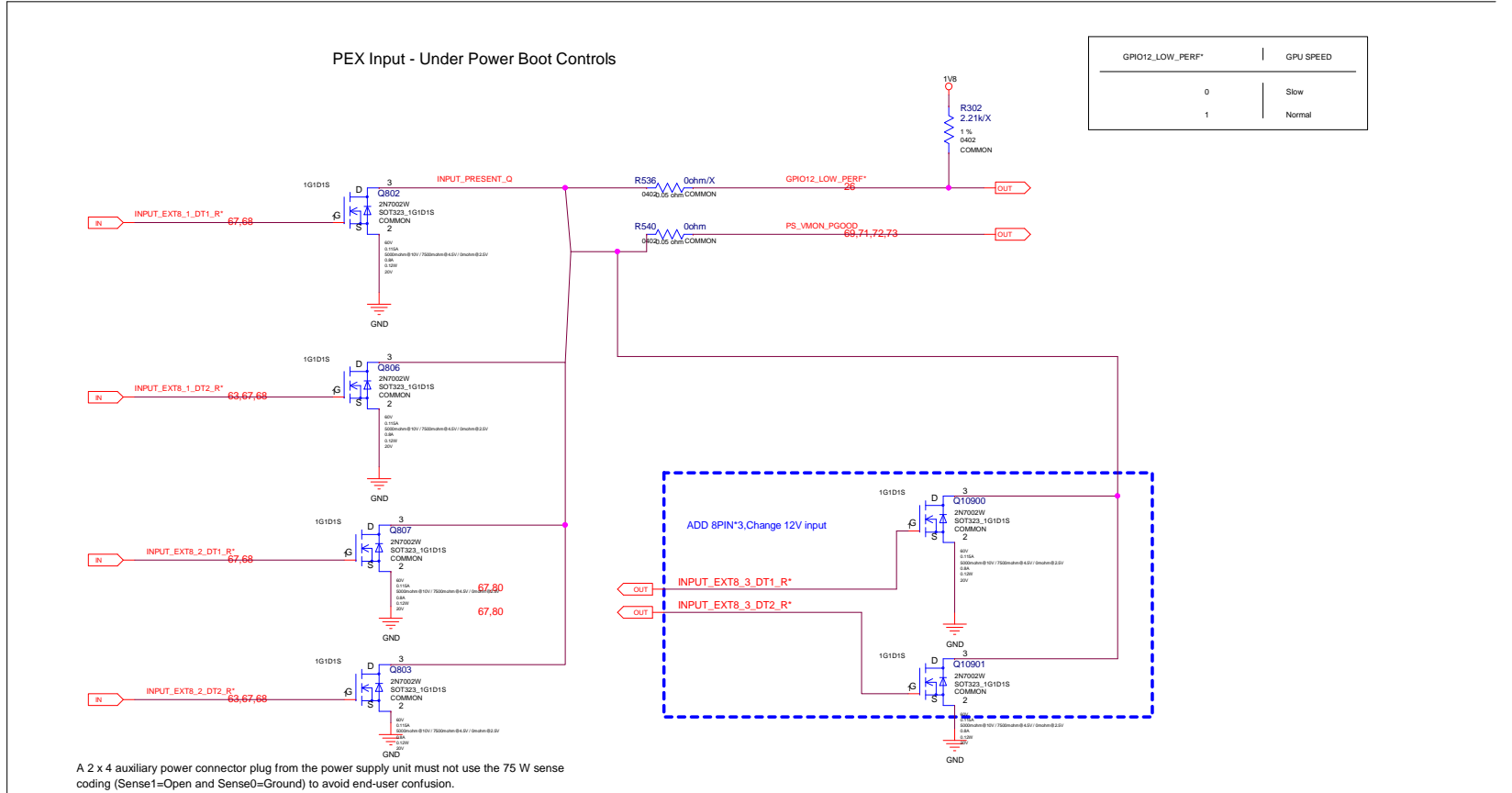
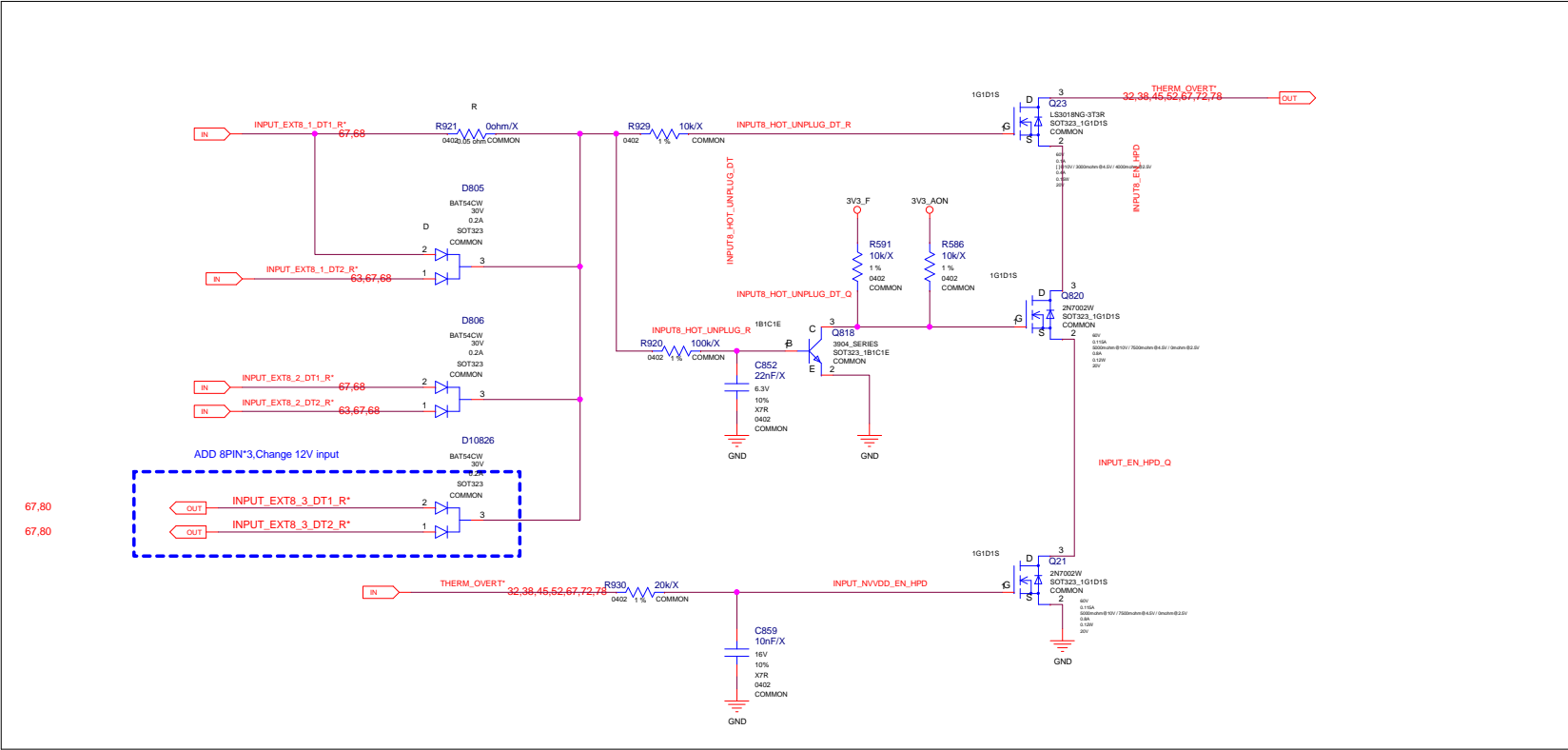
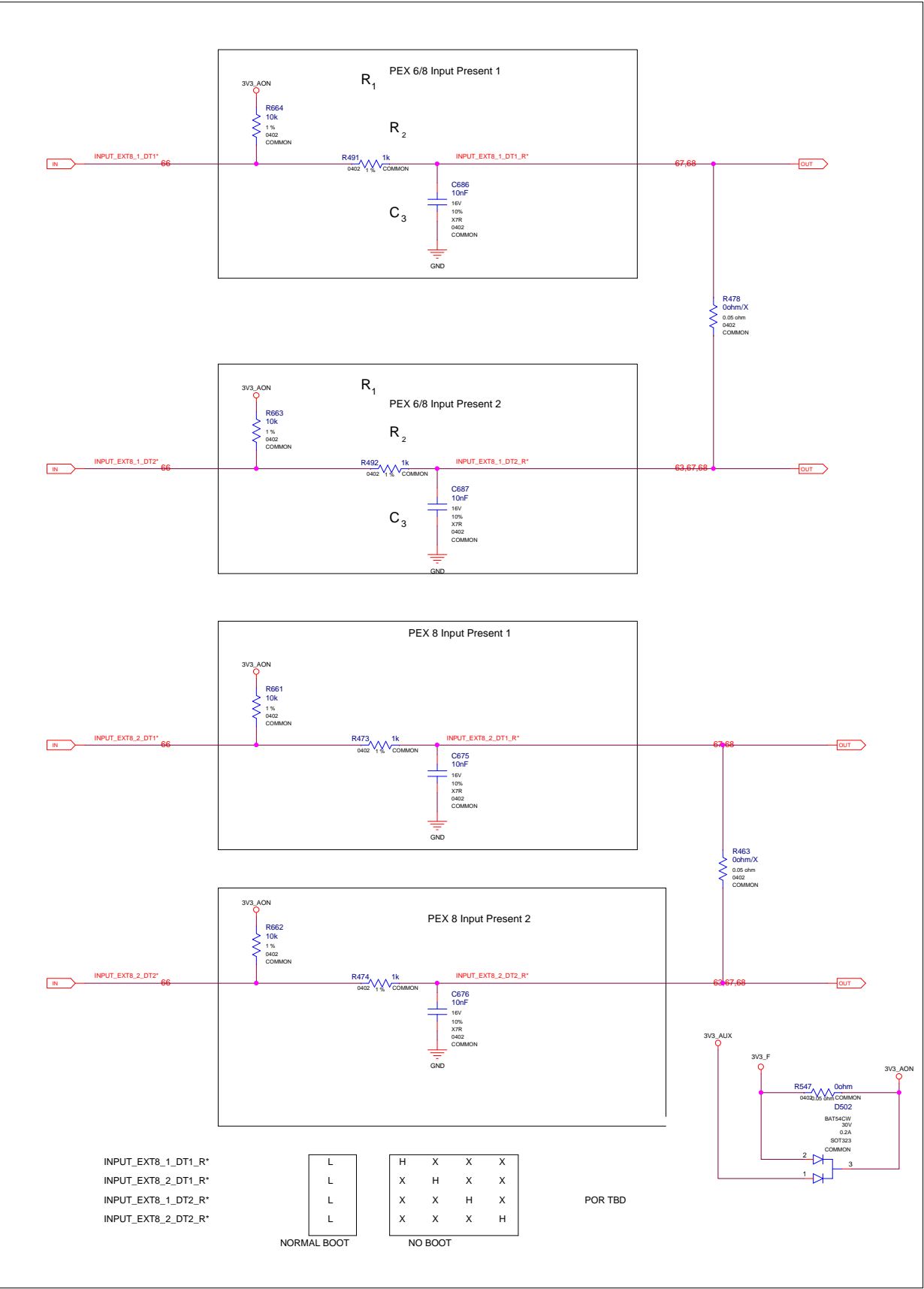


PEX\_12V INPUT - 66W



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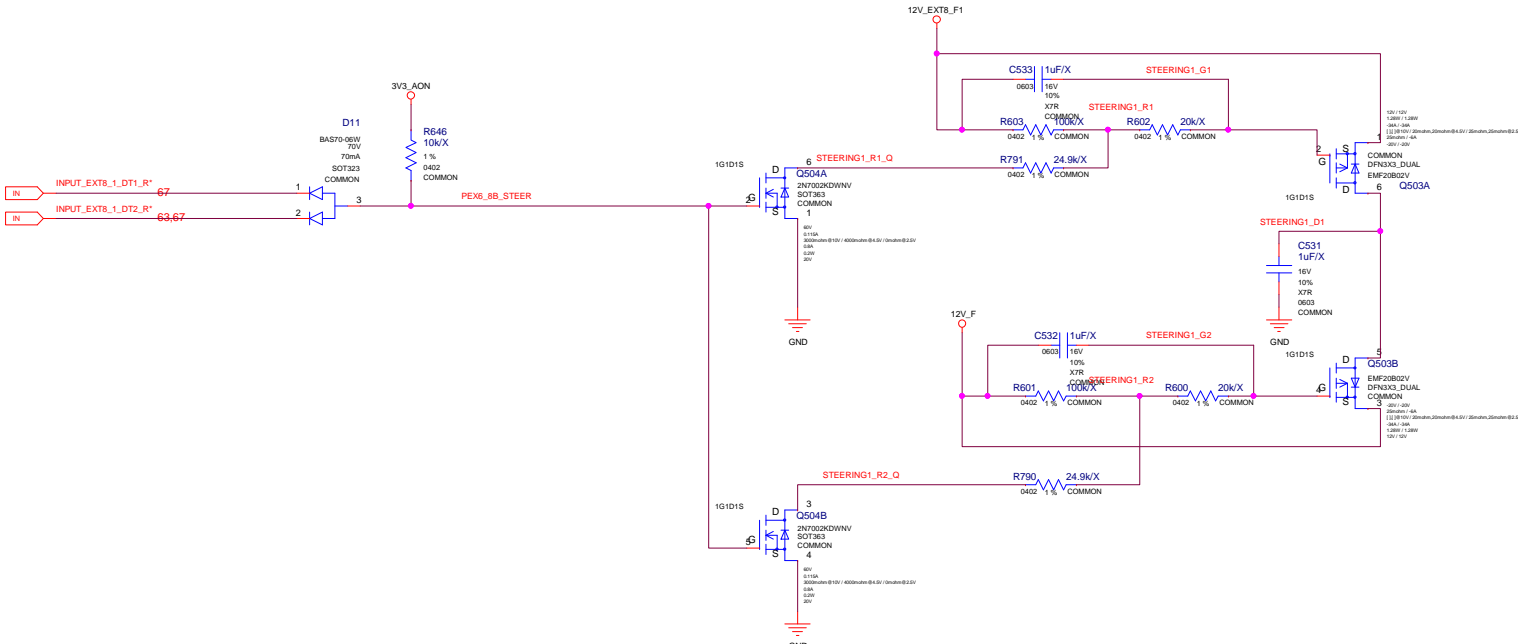
PS: 12V Current Steering & Hot Unplug Detect



PS: Discrete Steering

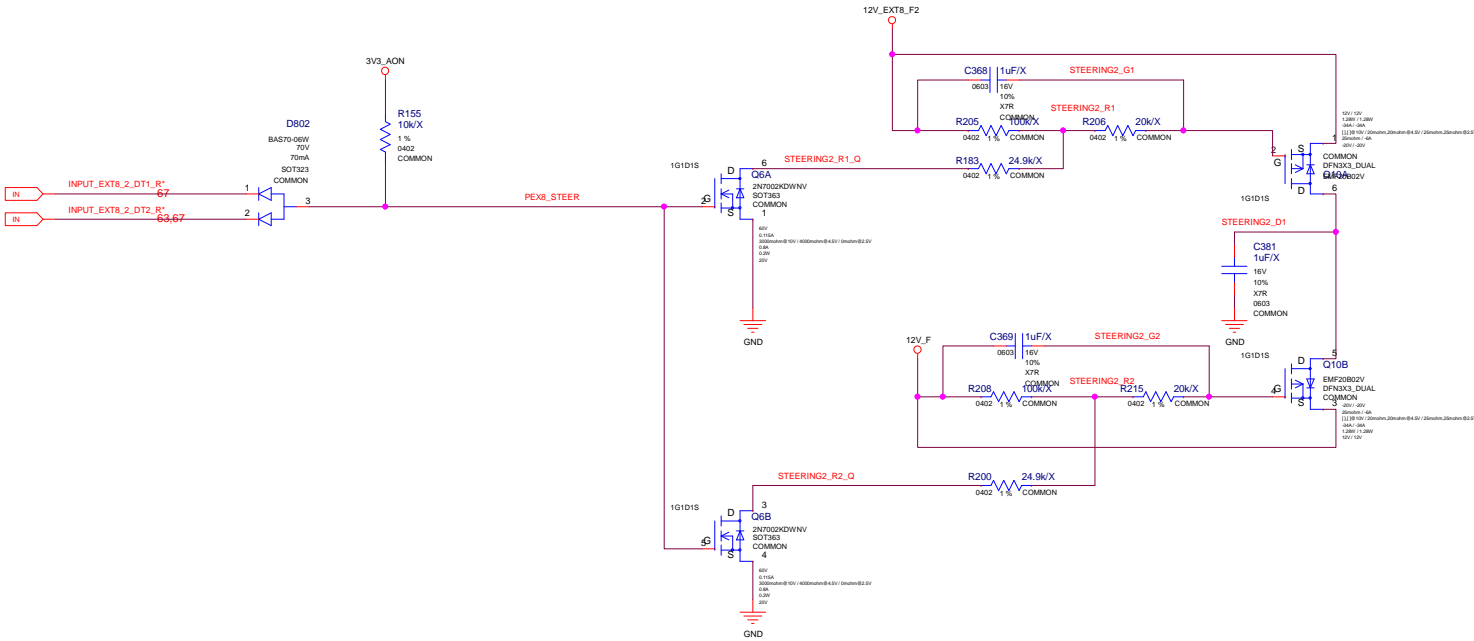
12V CURRENT STEERING (UNDER POWER BOOT):

PEX12V AND 12V\_EXT8\_F1



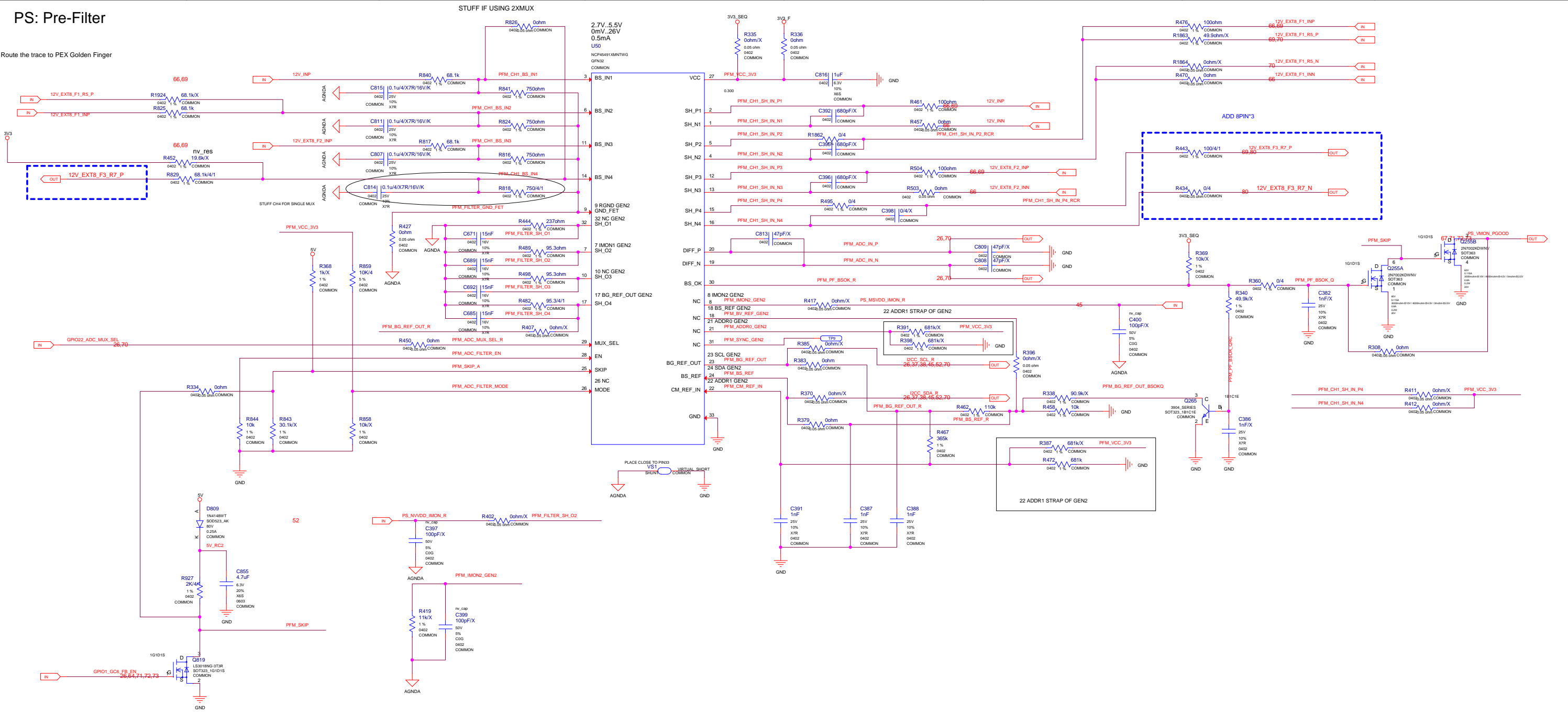
NO STUFF BY DEFAULT REF ONLY

PEX12V AND 12V\_EXT8\_F2



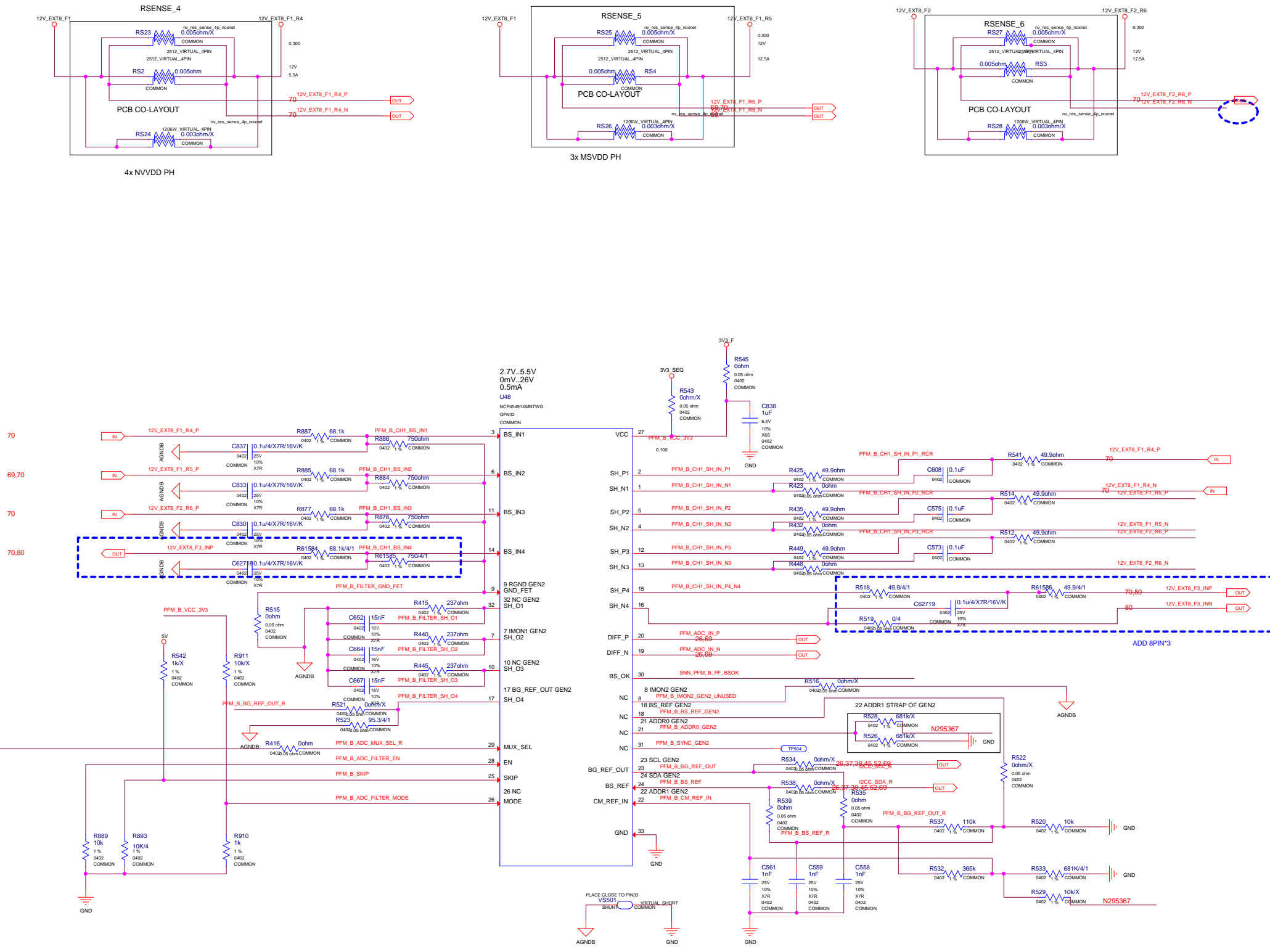
PS: Pre-Filter

Route the trace to PEX Golden Finger



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PS: Pre-Filter B



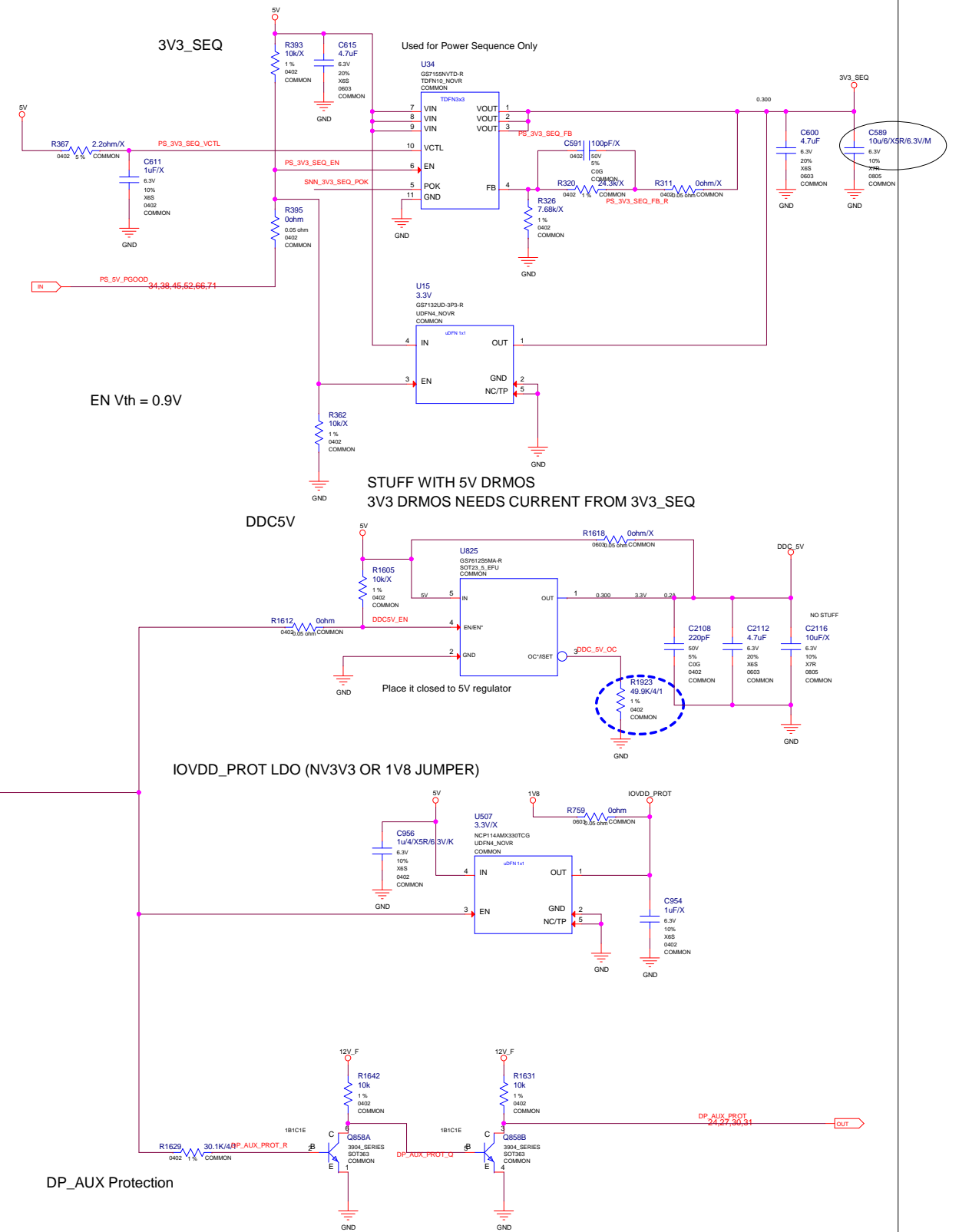
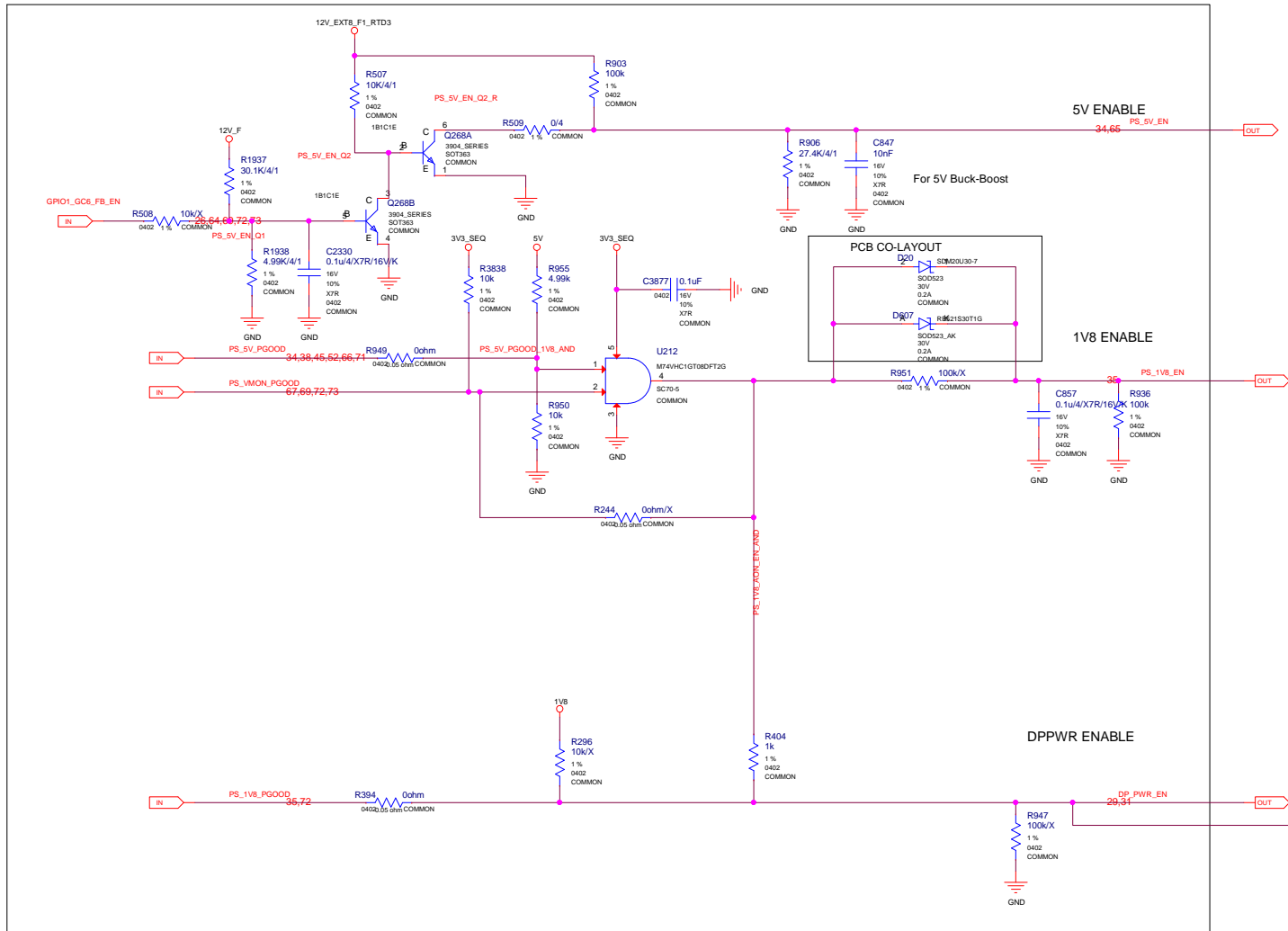
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PAGE DETAIL

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PS: Pre-Filter B			
Size	Document Number	Rev	
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Date:	Monday, September 28, 2020	Sheet	70 of 80

SEQUENCE:5V,1V8,3V3\_SEQ ENABLE



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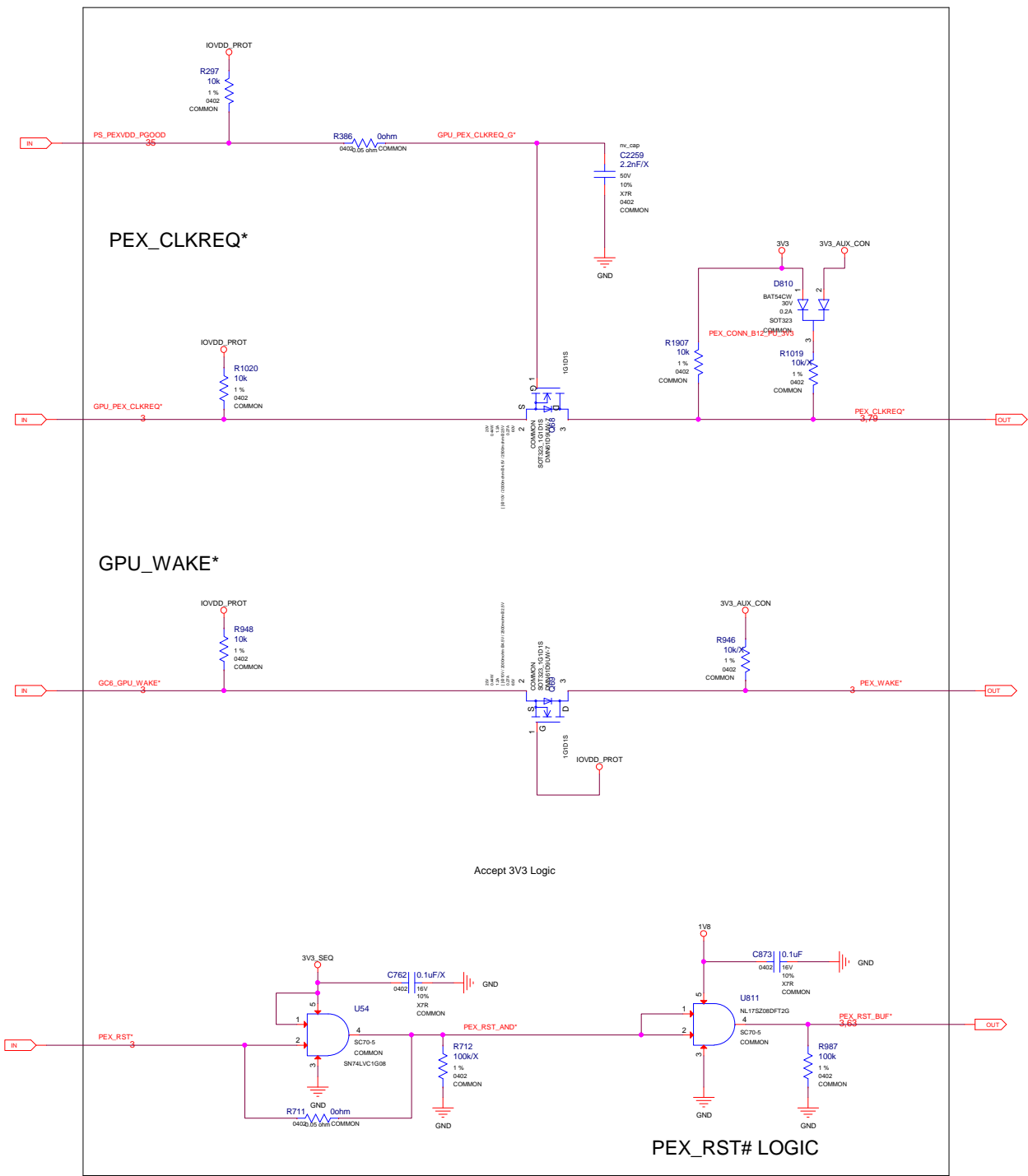
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Size	Document Number		
Custom	GV-N3080AORUS X-10GD		
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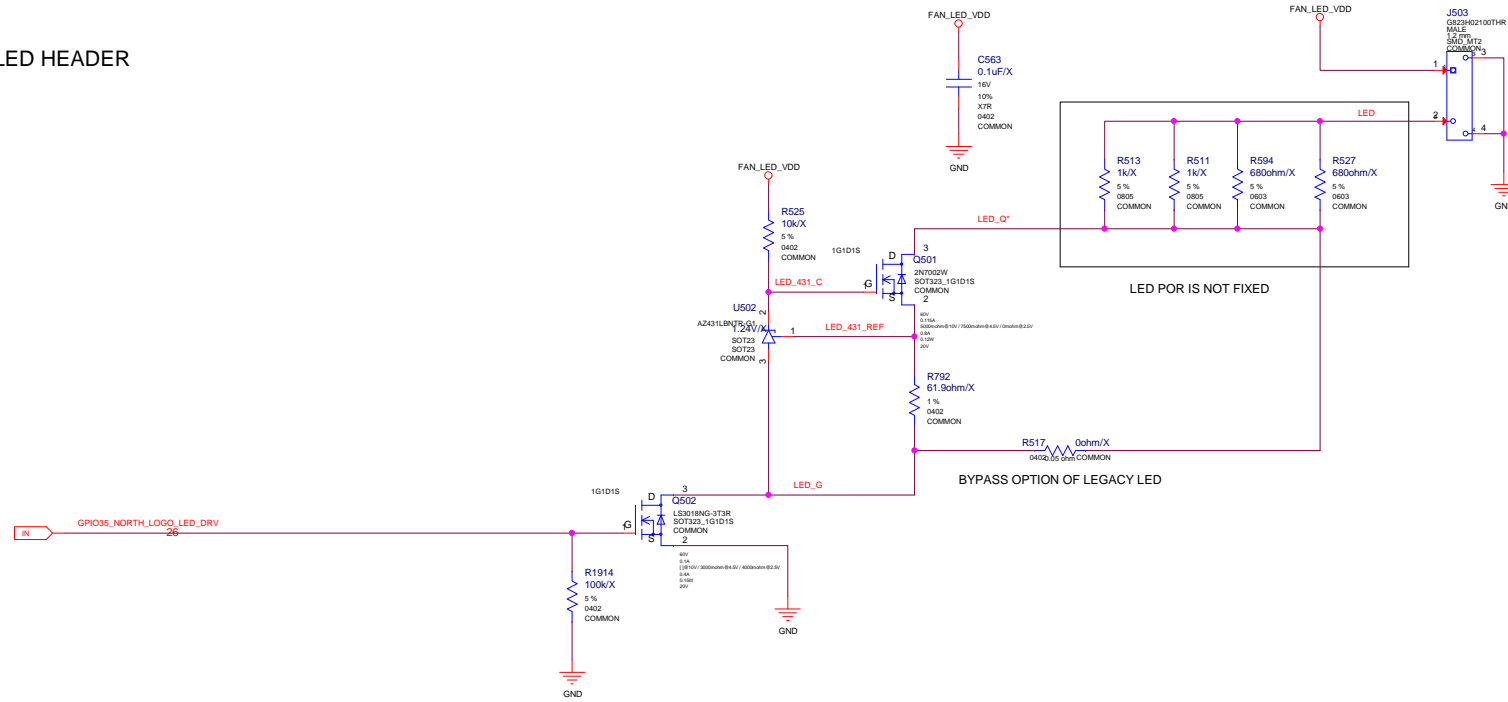
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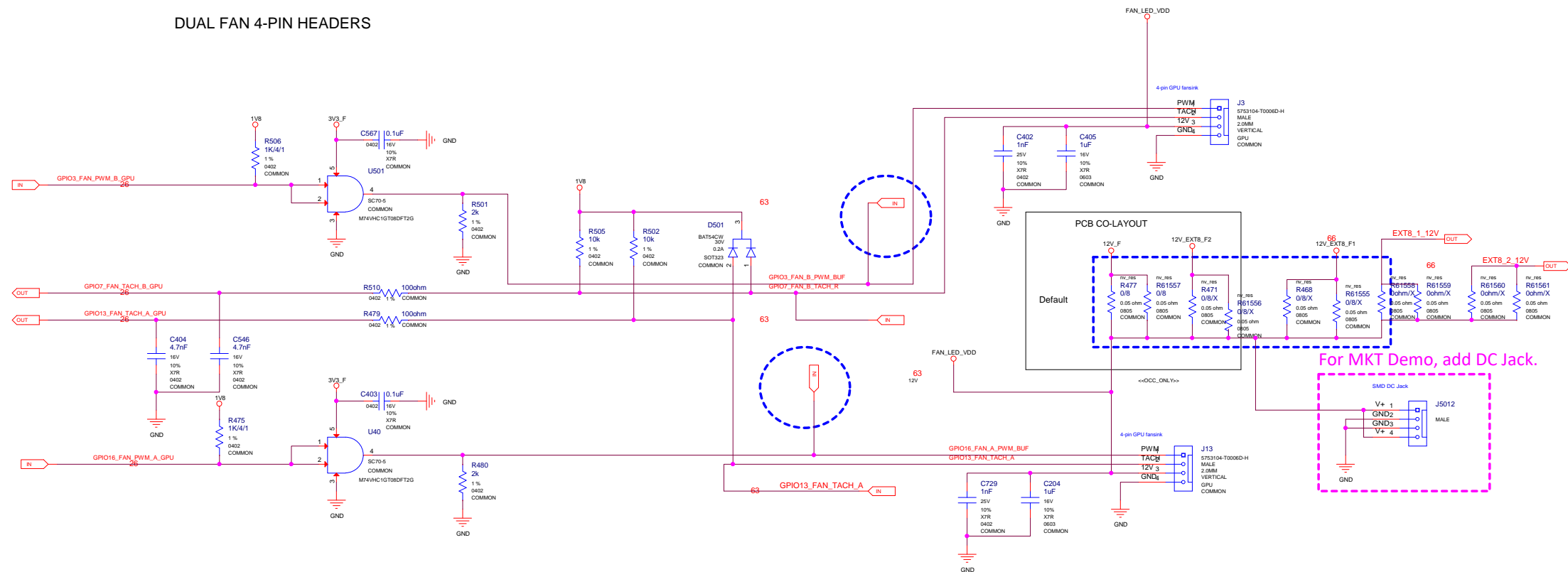
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MISC: LED & FAN

## 2-PIN LED HEADER

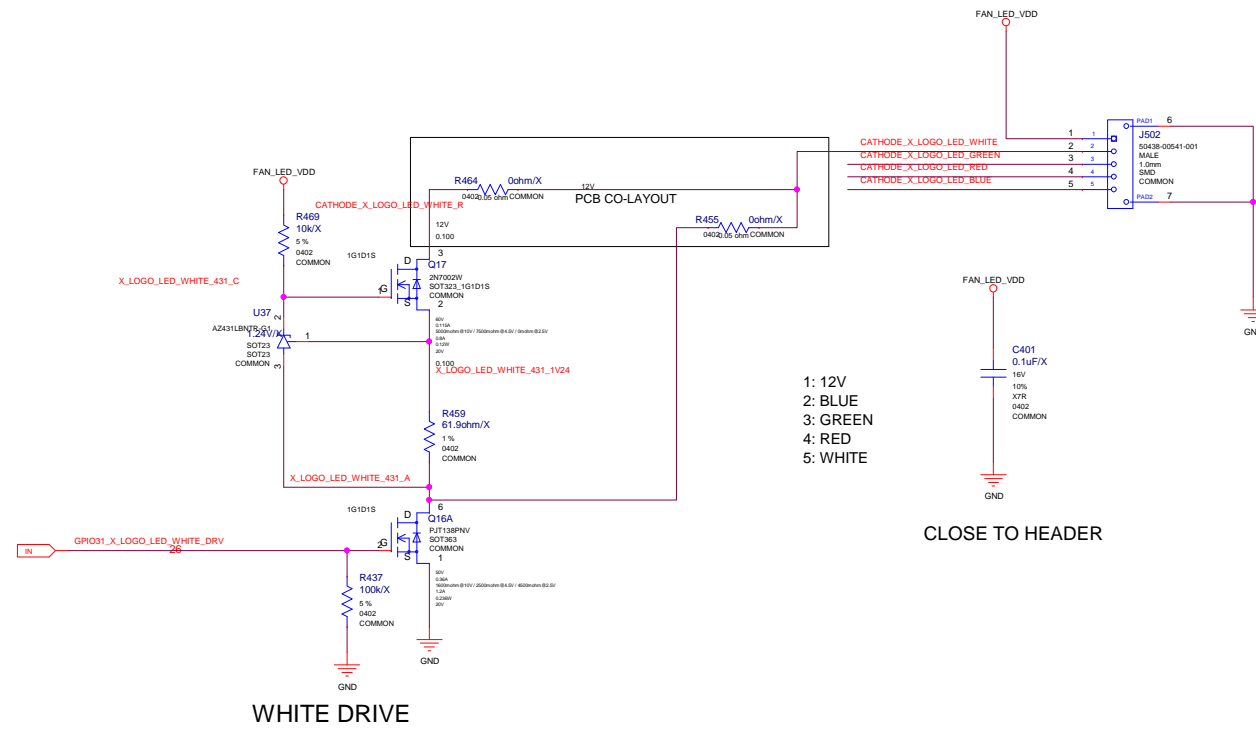


### DUAL FAN 4-PIN HEADERS

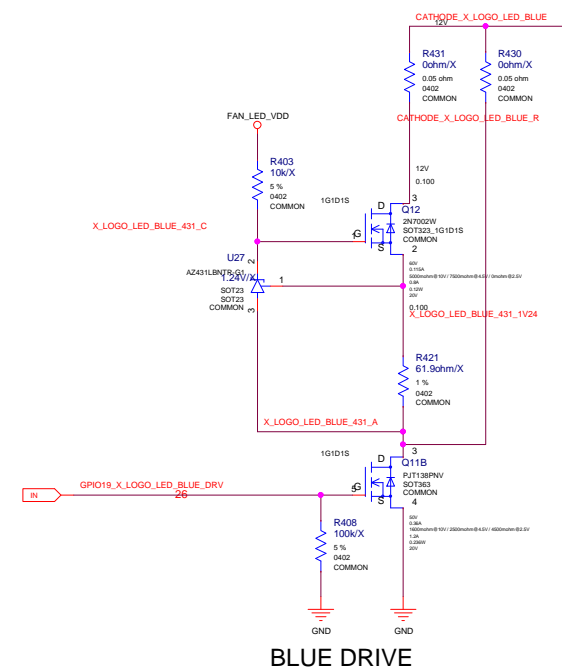
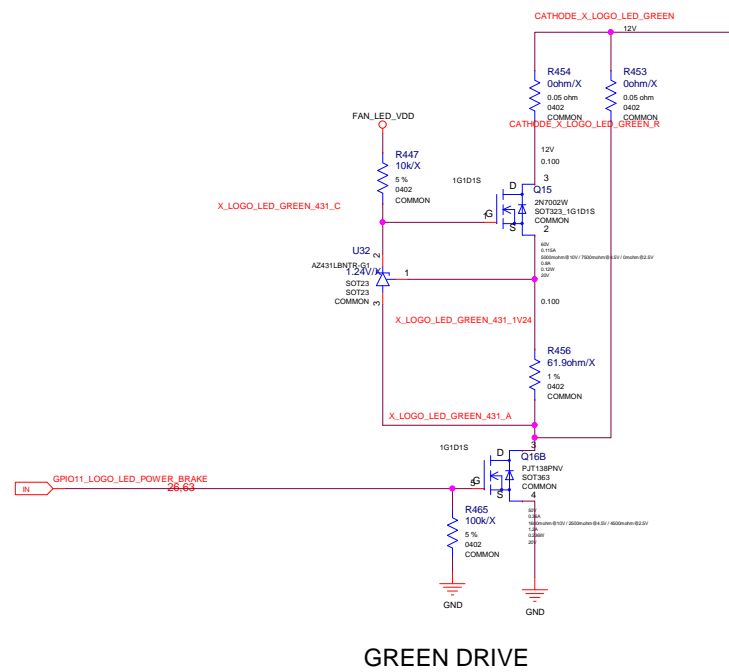
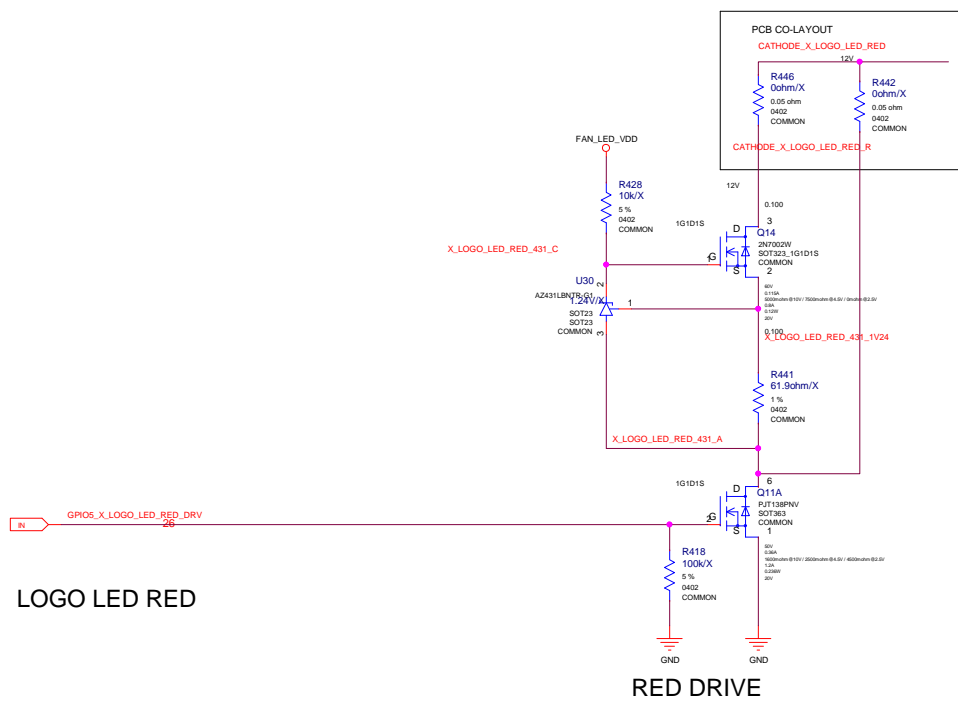


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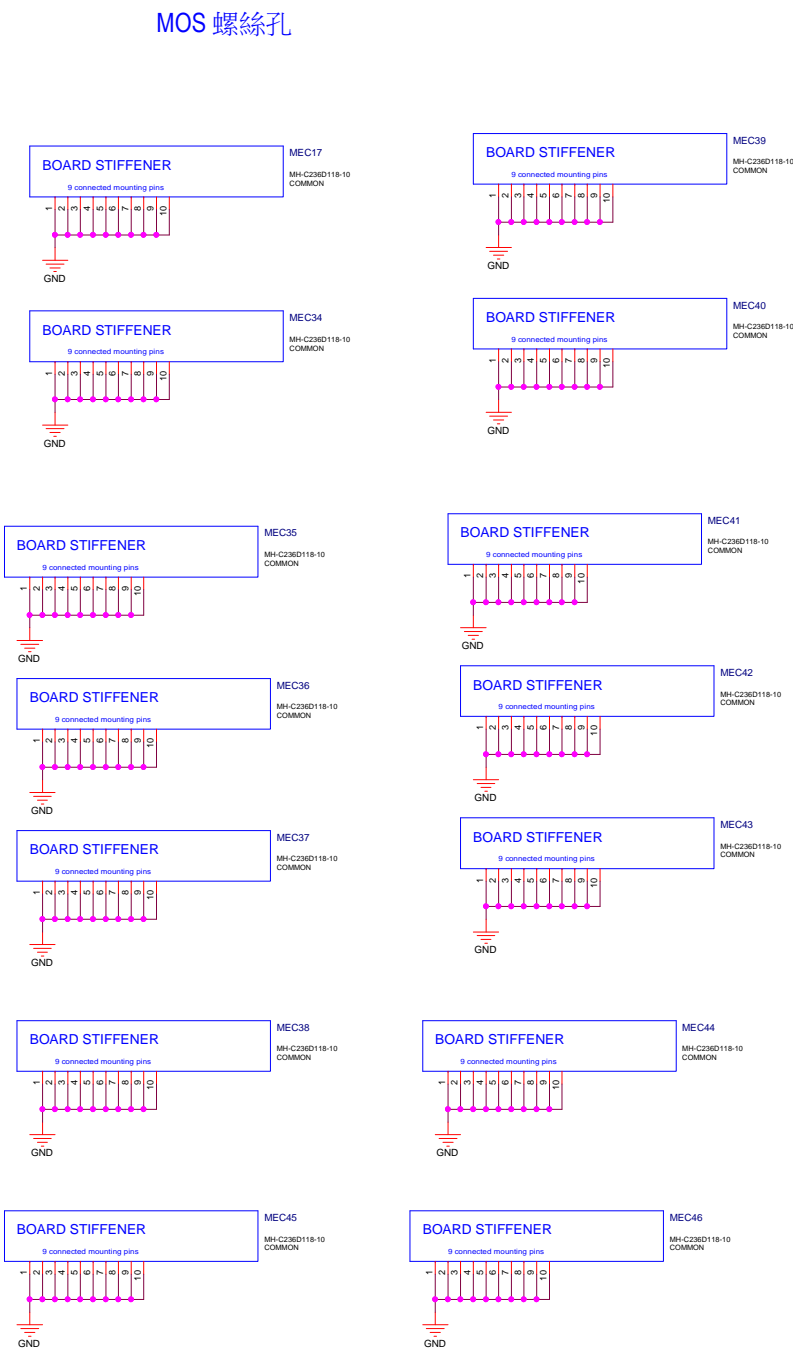
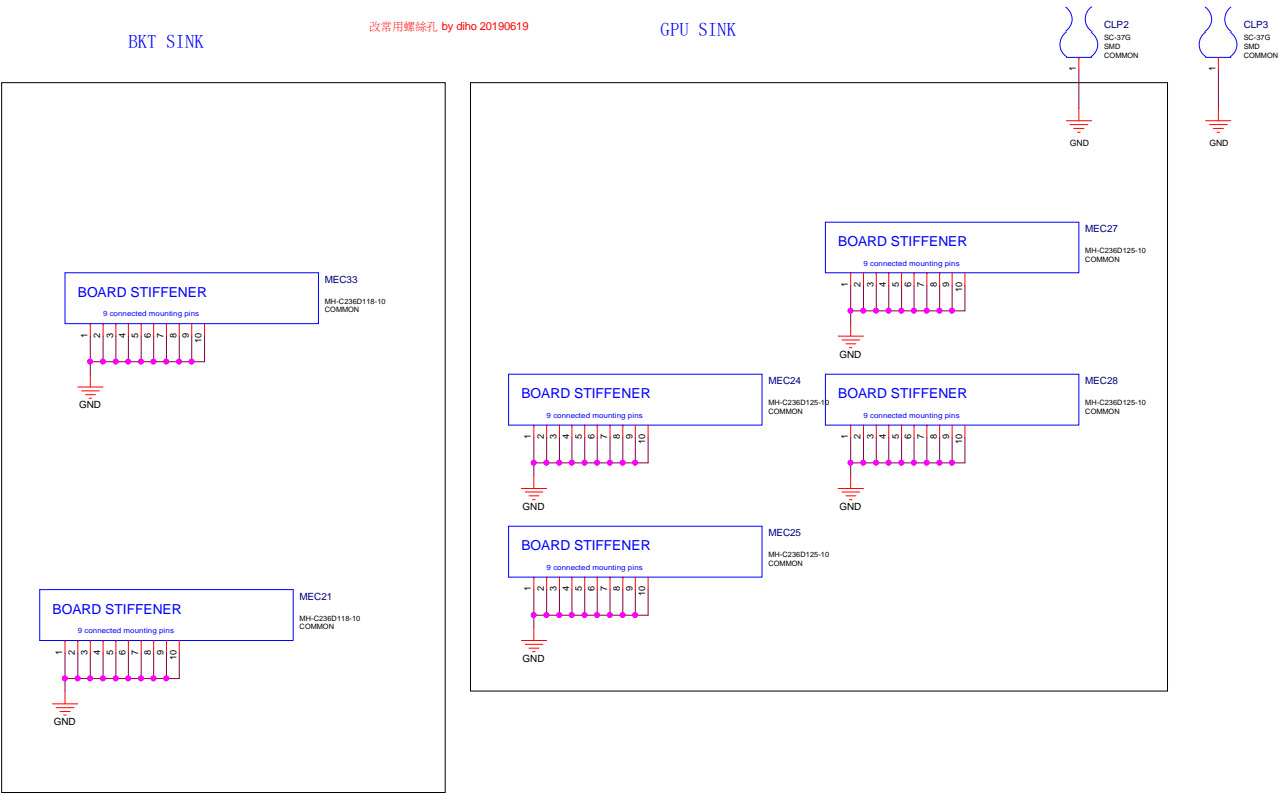
## MISC: RGBW LED REF



CONNECTOR SIZE TO FIT LAYOUT  
ALL CIRCUIT NO STUFF BY DEFAULT  
ALINGN WITH PASH  
IF ADDITIONAL POWER CONSUPTION R  
NEEDED, IT SHOULD BE ON LED MOD.

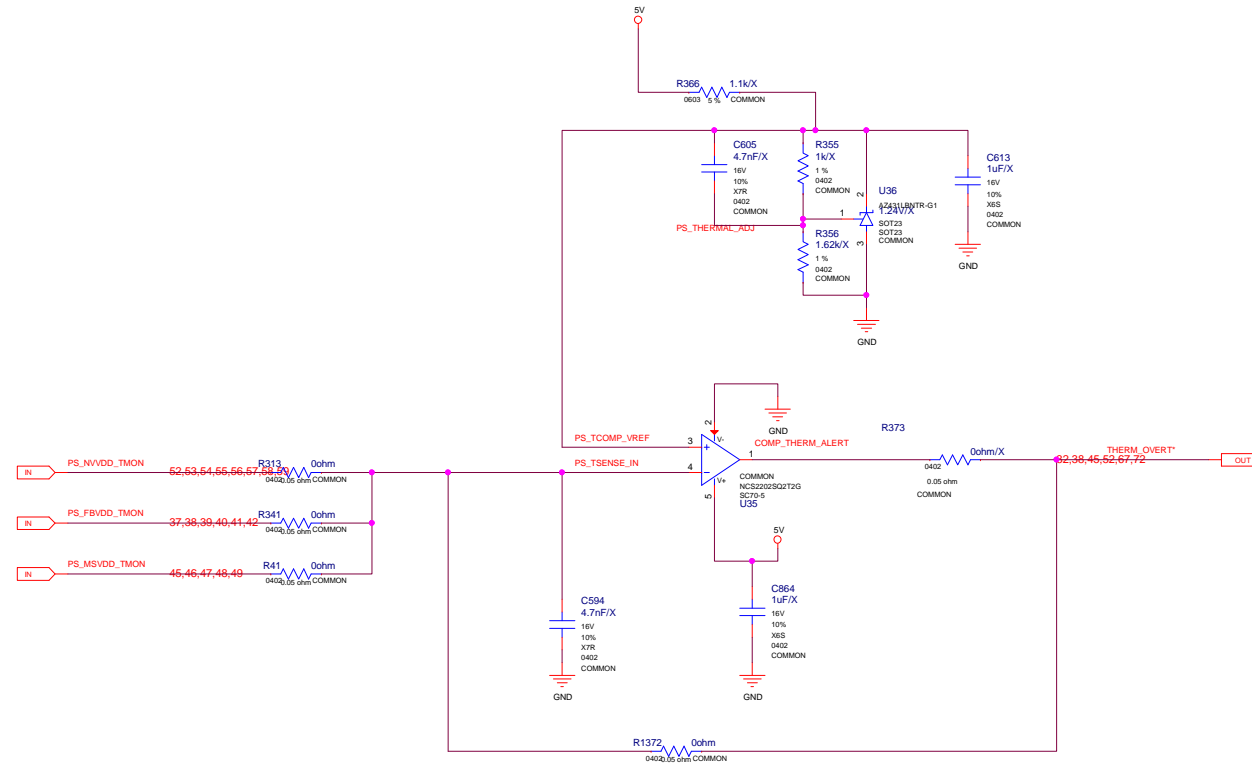


Mechanical: Mounting holes



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## VR THERMAL PROTECTION





PCI TERM

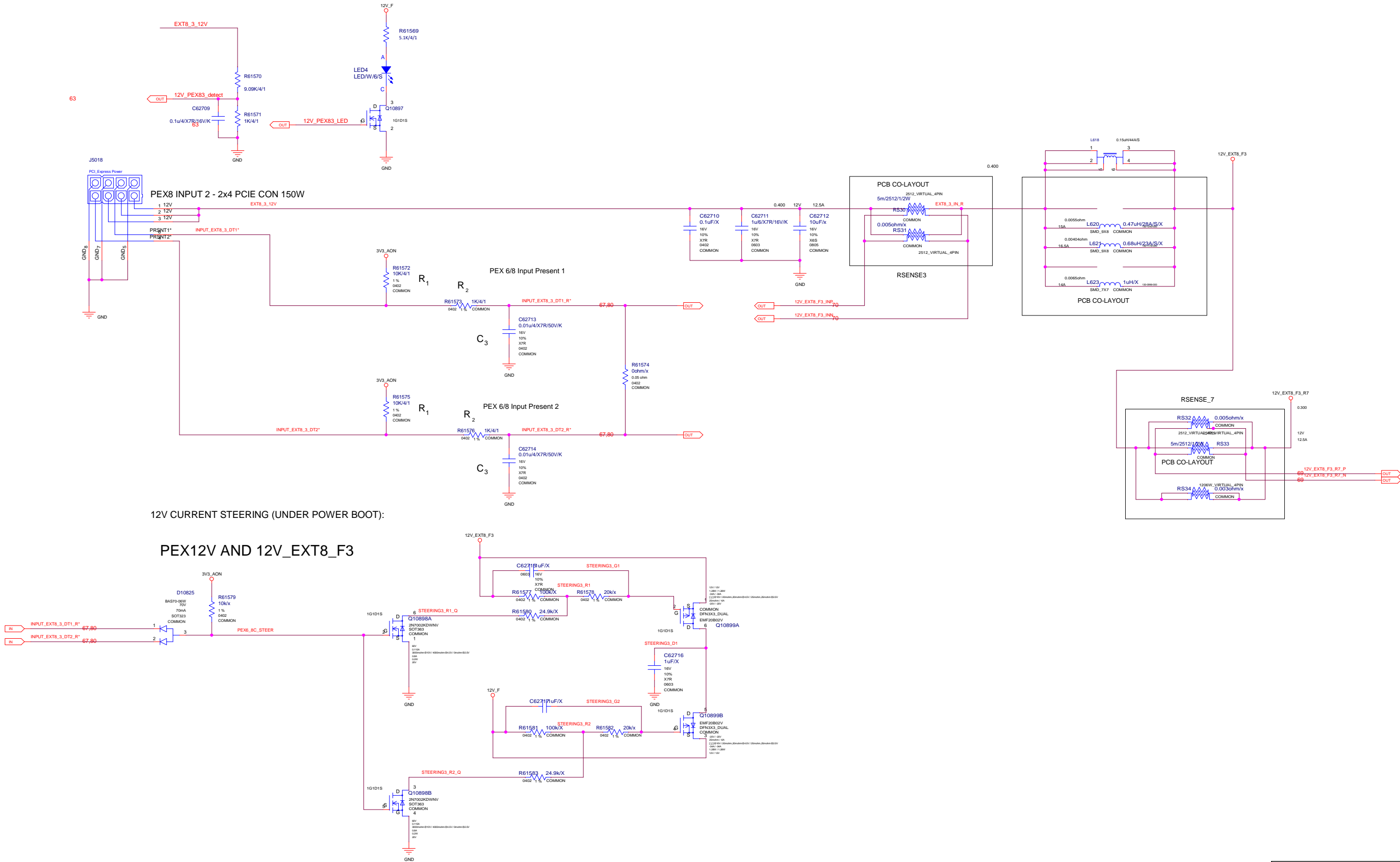


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PCIE TERM

GIGABYTE			
Title PCI TERM			
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